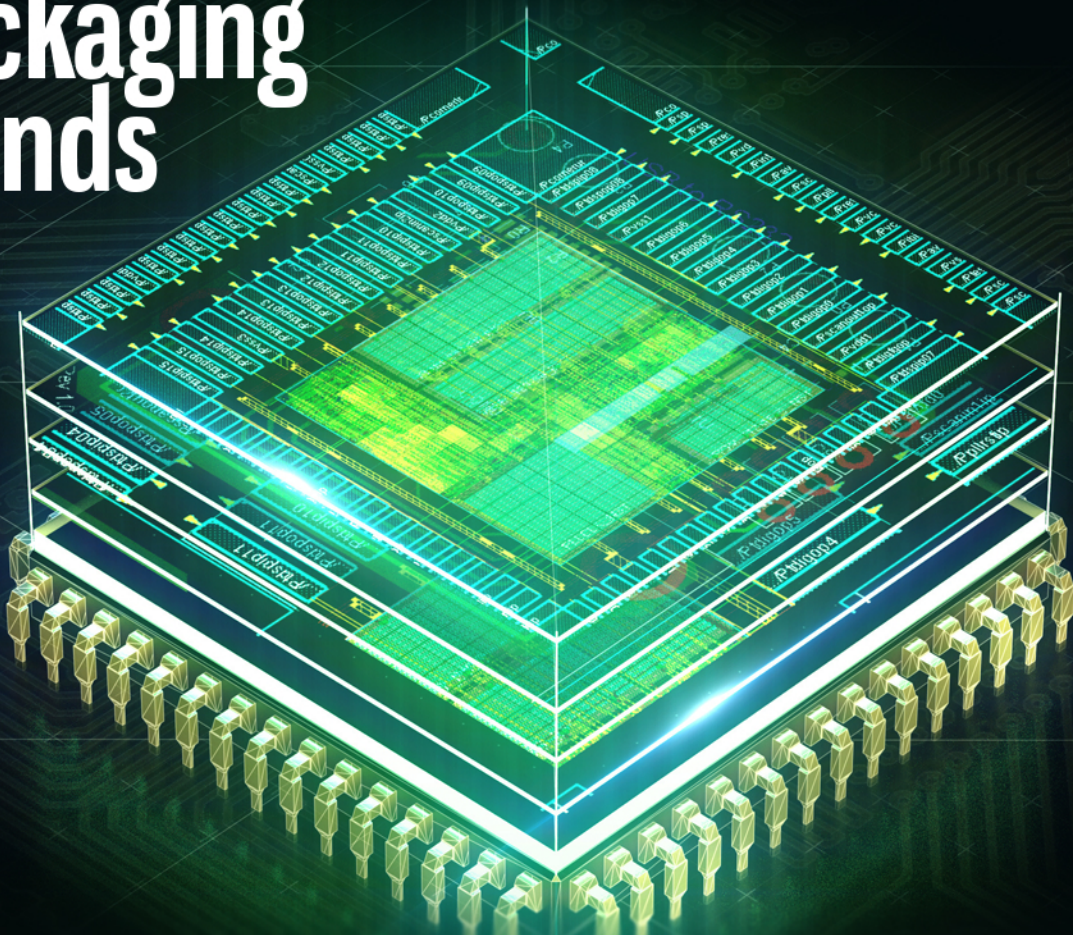


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## Packaging Trends





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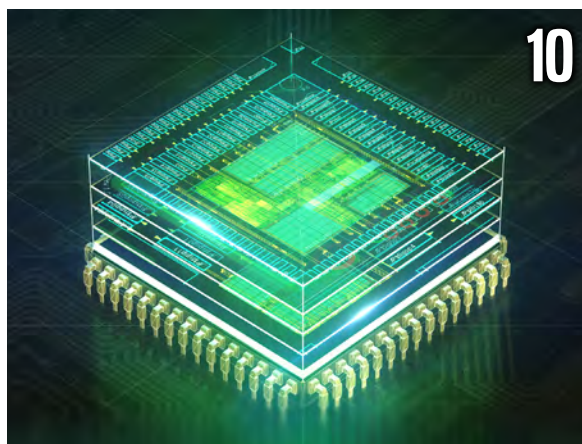
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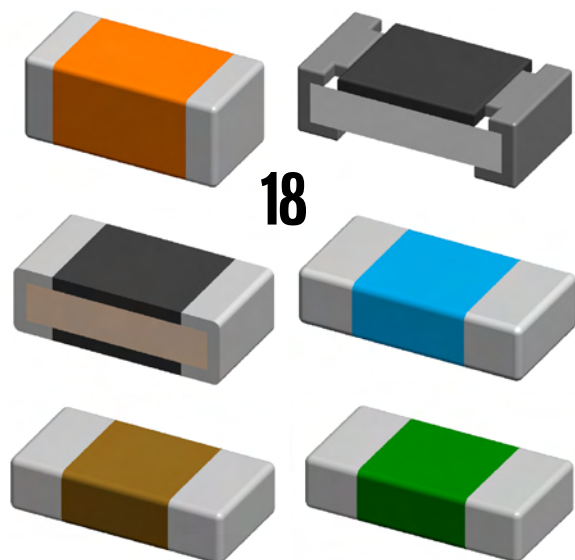
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## M A G A Z I N E



## Packaging Trends

Over the past 60 years, packages have continued to evolve, and shrink. The transistor outline “metal cans” of the 1950s would look out of place today. Some packages are no bigger than the period at the end of this sentence, complete with their own “inhalation warning.” Now, more types of packages than ever before that can be mounted on today’s PCBs. But package design is more complex than ever, too.



10

**Chuck Bauer  
Discusses  
the Future of  
Packaging**

by I-Connect007  
Editorial Staff



18

**Standard PCB Component  
Families, Part 1**

by Tom Hausherr

28

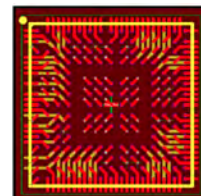
**PCB Design Challenges:  
A Package Designer’s Perspective**

by Bill Acito

34

**BGA Fanout Routing  
Overview**

by Christian Keller



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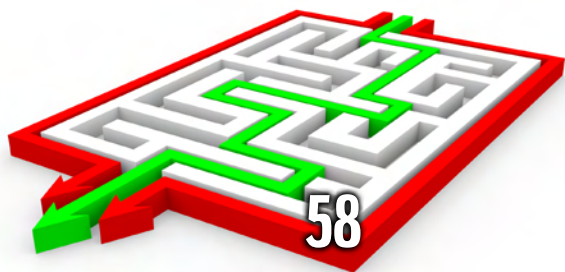
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- 9** Amkor SmartPackage Speeds Accurate Design and Verification
- 26** Quantum Chains in Graphene Nanoribbons
- 33** Quick Memory
- 38** New 3D-Printed Device Could Help Treat Spinal Cord Injuries
- 51** Smart Homes Open New Approaches and Business Models for Healthcare Delivery
- 55** EMA Expands Library with Power Integrations EDA and MCAD Models
- 62** Free Webinar: Panelization with the Xpedition Flow
- 68** Novel Approach to Coherent Control of a Three-Level Quantum System

**74 Career Opportunities**

**80 Events Calendar**

**81 Advertiser Index & Masthead**



## 58 The Impact of PCB Dielectric Thickness on Signal Crosstalk

by Chang Fei Yee

## 64 Moving From 28 Gbps NRZ to 56 Gbps PAM-4: Is it a Free Lunch?



## 8 The Whole Package

by Andy Shaughnessy

## 42 It's a Material World



## 48 Transitioning from FR-4 to High-Frequency Materials, Revisited

## 52 Testing Time for Resins



40 PCB007

56 MilAero007

70 Top 10 PCBDesign007



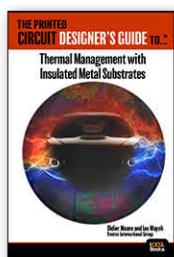
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# The Whole Package

## The Shaughnessy Report

by Andy Shaughnessy, I-CONNECT007

When we started planning this issue, I found an interesting tidbit of information: Electronics packaging predates the printed circuit board. Most electronics history buffs seem to agree that the Braun Tube of 1897, the forerunner of the cathode ray tube, was the first true electronics package.

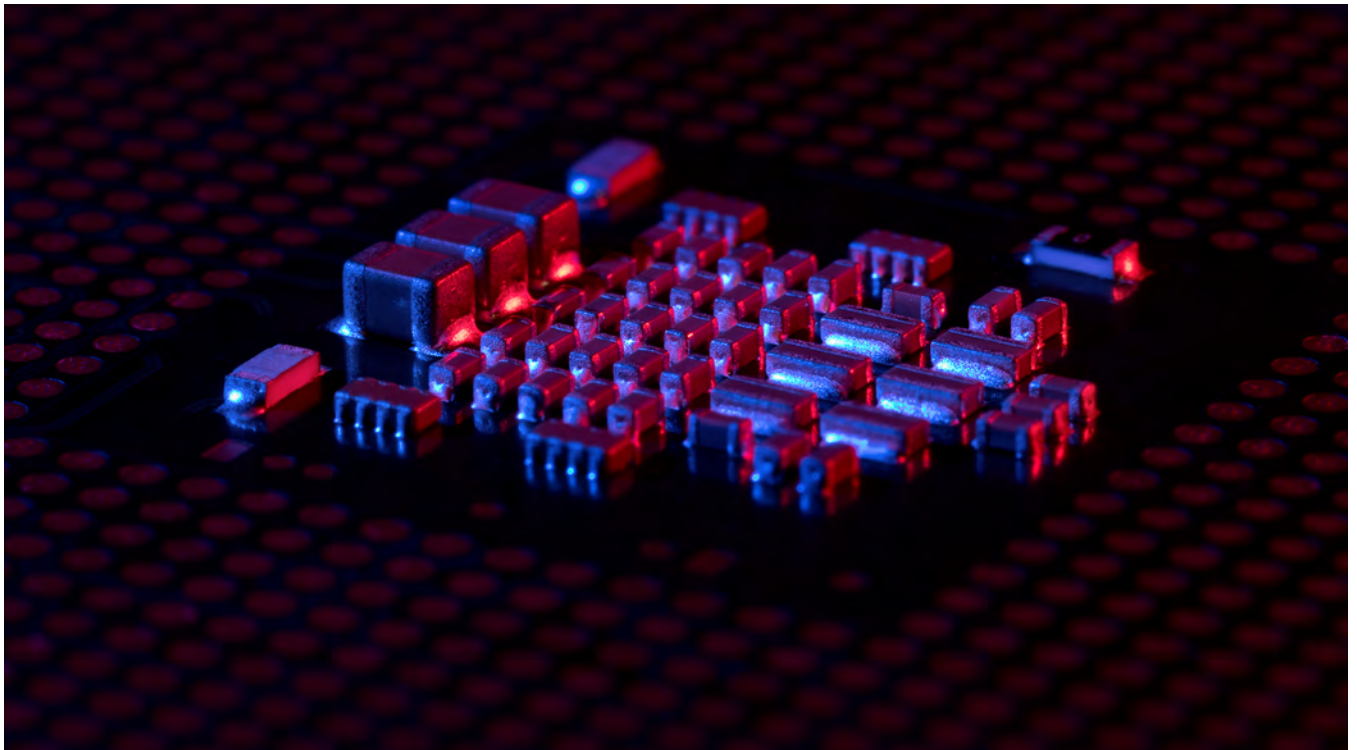
Aren't you glad you don't have to place a glass package on your next board? (But glass may be making a comeback, this time as an interposer in packaging. More on that later.)

Over the past 60 years, packages have continued to shrink. The transistor outline "metal cans" of the 1950s would look out of place today. Some packages are no bigger than the period at the end of this sentence, complete with their own "inhalation warning."

Now, more types of packages than ever before that can be mounted on today's PCBs. It can be hard to keep this alphabet soup of packages straight: QFN, QFP, SOT, TSSOP, PDIP, WLCSP, BGA, FPBGA, SOIC, PoP, COF, WLP, FOWLP, and a few dozen more, I'm sure.

Designers wind up having to deal with these packages, and each package has its own pros and cons. For instance, the BGA is known for its densely packed array of pins, with large BGAs often boasting 3,000 pins, or more. But routing a 3,000-pin BGA can be a mind-numbing task for a PCB designer.

Luckily for designers, most of today's EDA tools feature some package design capabilities, with package design integrated into the usual PCB layout tool. But the package landscape



continues to shift, and packages are likely to keep getting smaller and denser as technologies such as IoT and 5G take hold.

For this issue of *Design007 Magazine*, we asked a variety of package experts to share their opinions about the component package trends of today and tomorrow, as well as some of the drivers behind this evolution. In our first feature interview, Chuck Bauer of TechLead Corporation explains some of the trends he's seeing in packages, such as fan-out wafer-level and 3D packaging, and the need for new packaging technologies to be scalable and cost-effective. Next, Tom Hausherr provides one of the most exhaustive collections of standard PCB components that I've seen, complete with package size codes and dimensions.

Bill Acito of Cadence Design Systems discusses the many challenges faced by PCB designers and packaging designers, and he offers some new tips and tricks for dealing with ever-denser packages, not to mention time and budget constraints. And Christian Keller of Altium provides an overview of BGA fanout and escape routing, including techniques for using stacked and staggered microvias, blind vias, and via-in-pads.

We have columns by our regular contributors, including Barry Olney of iCD, John Coonrod of Rogers Corporation, and Alistair Little of Electrolube. And we also have articles by Chang Fei Yee of Keysight Technologies and Yuriy Shlepnev of Simberian.

It's hard to believe that the summer is drawing to a close, and show season is right around the corner. I hope to see you at PCB West in September.

If you aren't already a subscriber, [click here](#) to be sure you don't miss any of our magazines and newsletters.

See you next month! **DESIGN007**



**Andy Shaughnessy** is managing editor of *Design007 Magazine*. He has been covering PCB design for 18 years. He can be reached by clicking [here](#).

## Amkor SmartPackage Speeds Accurate Design and Verification

Amkor Technology, Inc. announced it has partnered with Mentor to release Amkor's SmartPackage™ package assembly design kit (PADK), the first in the industry to support Mentor's high-density advanced packaging (HDAP) design process and tools. Amkor's award-winning high-density fan out (HDFO) process can now be used in conjunction with Mentor's software to deliver early, rapid and accurate verification results of advanced packages required for Internet-of-Things, automotive, high-speed communications, computing and artificial intelligence applications.

"Amkor leads the way in HDFO technology for OSAT companies, and with the rise of complex ICs with multi-die packages, we prioritized the creation of Mentor-based PADKs to significantly reduce cycle time," said Ron Huemoeller, corporate vice president, Research & Development, Amkor Technology. "Since the Mentor flow includes Calibre, the golden sign-off tool for the fabless ecosystem, our customers can easily close any physical verification issued for their entire solution." AJ Incorvaia, vice president and general manager of Mentor's BSD division continues, "By providing a fully validated PADK for Amkor's HDFO process for Mentor's proven HDAP tool flow, customers can more easily transition from classic chip design to 2.5 and 3D solutions."

The complex and compact design of devices for today's smart applications is driving the need for sophisticated packaging techniques such as heterogeneous integration and Advanced System-in-Package. These solutions combine one or more ICs of different functionality with increased I/O and circuit density in 2.5D (side-by-side) and 3D constructions. The graphic environment features robust data and is straightforward to use before and during the implementation of physical design, resulting in faster sign-off and fewer verification cycles.

Source: Amkor.com



# Chuck Bauer Discusses the Future of Packaging



## Feature by I-Connect007 Editorial Staff

When we decided to cover the future of PCB packaging, we knew we would have to interview Charles Bauer, Ph.D., owner of TechLead Corporation. For over 35 years, Chuck has been a pioneer in electronics packaging, from 3D and system-in-package to multichip modules and nano technology. He's a frequent speaker at events like SMTA International, ICEP Japan and ESTC in Europe. He also founded the Pan Pacific Micro-electronics Symposium.

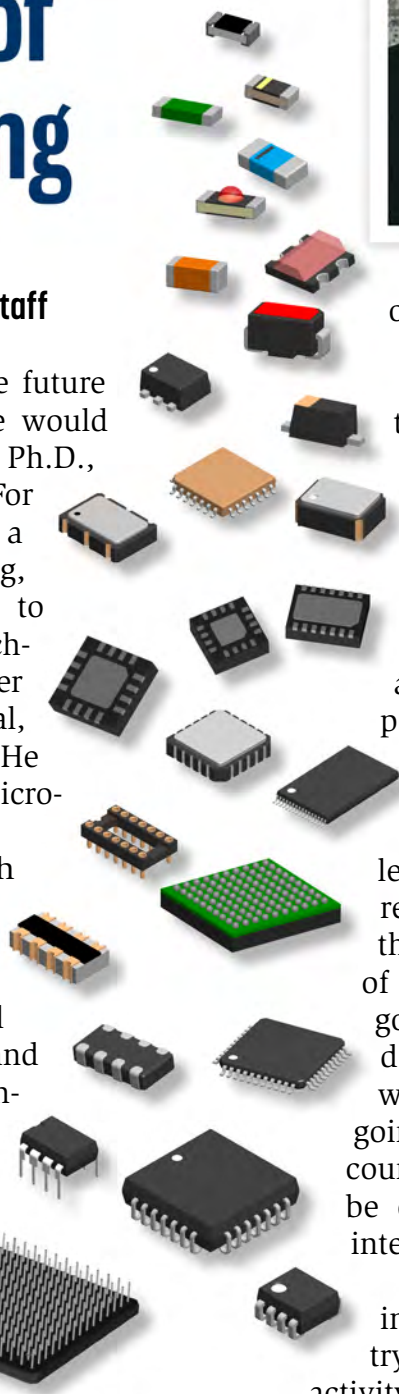
Chuck recently spoke with Happy Holden, Andy Shaughnessy and Barry Matties about current trends in packaging, the need for product designers and manufacturers to communicate, and why no matter how cool the technology is, cost is still king.

**Happy Holden:** Chuck, some of the big trends are 3D packaging and wafer-level packaging. Wafer-level packaging is of interest to a lot

of our readers because the organic package substrate is a leading edge for circuit board technology. With this wafer-level packaging push, it wants to be finer and finer pitch. What does that do to the assembly, Chuck?

**Charles Bauer:** First, I think that wafer-level packaging is really a misnomer because wafer-level packaging isn't really being done so much at the wafer level anymore. There's fan-in, wafer-level packaging, which is indeed a wafer-level packaging approach. That's relatively limited today, and I think that some of the barriers in terms of interfacing with circuit boards are going to inhibit that technology. It doesn't mean it can't be done or won't be done; it just means it's going to be inhibited in terms of pin-count because their pitch is going to be constrained by the next level of interconnection.

There are countervailing trends in the assembly side of the industry, where we're seeing a lot more activity going on in the area of nano



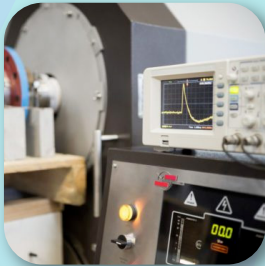


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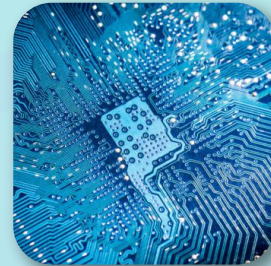
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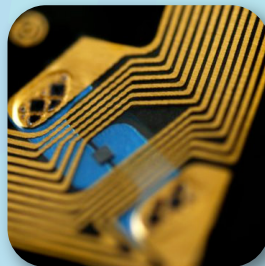
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assembly. For example, about four years ago we did a project that had a wafer-to-wafer connection. We used a nano silver technology to join a CMOS pre-amplifier chip directly to an indium phosphide avalanche photo diode. We were connecting those two chips to each other, and we were doing it on a 32-micron pitch with 6-micron pillars. Today, they're down to about 22-micron pitch, and the goal is to get it to 15-micron pitch.

IBM Zurich has been very active in using nano copper as the bonding medium to assemble fine-pitch packages down to about 40-micron pitch onto printed circuit boards. I think that there will necessarily be materials development that will allow us to achieve those finer pitches. How fine a pitch we have to go to is a different question. As we go to too fine a pitch, what happens to the printed circuit board? I do think that, especially in the kinds of products that are going to use these super fine pitch devices, you're starting to see a trend toward more and more flex and flex rigid type structures.

The one area where those packages are going to be a big player is in areas such as IoT. No other markets are big enough to justify processing of devices at a panel level like that, because most of the technologies that we use, and most of the designs that we use, just don't use enough volume to justify putting together a panel processing line, when you look at the capacity.

We have to look at the market side of things as well—not just at the technology. I think what you'll find is that wafer-level packaging will continue toward finer pitches, but as the wafer-level packaging ties to technology, it is going to be for very specific applications, where

the volume justifies it. In those cases, they'll use a specialized substrate. With the general print circuit board market, obviously it is still going to have to advance, but the general circuit board market will continue, at least for the next decade or so, to be driven by leading-edge packages that are essentially trying to integrate multiple devices into a single package that can then be surface-mounted onto a circuit board.

Things like the video cameras for cell phones, for example, are classic 3D packages. They continue to evolve, although not very rapidly, because the solution seems to work pretty well. I'm not saying that there won't be millions of wafer-level packages mounted on printed circuit boards. But basically, wafer-

level packaging serves a niche market, admittedly a very large niche market, but I think the niche market has primarily been IoT and to a certain level the cell-phone market.

**Holden:** There's always more and more integration of silicon, and I believe that the system-in-package, SiP, is a bigger trend. As that trend moves on, you can reduce the number of flex circuits and things like that into a simpler construction.

**Bauer:** Yes, I hear you.

The real battle is going to be between what is more efficient, and not necessarily from a technical perspective, from the chip side, but more from a cost/performance analysis between system-in-package and further integration at the chip level. Obviously, Intel took the microprocessor forward a long way and integrated the video processor and that sort of thing into it. Everybody rang the death knell of the video processor, and yet today's top-end computers still have a separate video processor.

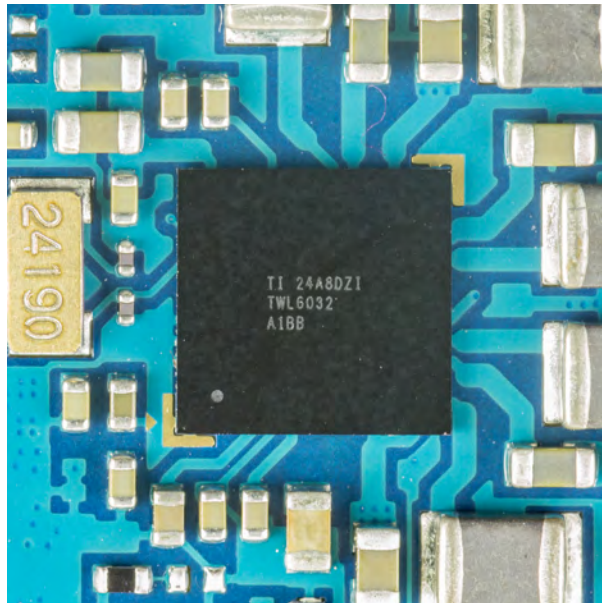


Figure 1: Texas Instruments wafer-level 155-pin WCSP, fully integrated power management with power path and battery charger. Image source: © Raimond Spekking, Wikimedia Commons

I think there's always a cost trade-off when you try to integrate too much into a chip, and if you do integrate too much, then the question is: Does that narrow the market for that particular device? I think we all know that for chip makers in general, if there's no volume, there's no opportunity. The memory guys know that in spades. That's why we don't have 128-bit wide memories put into switcher routers for the internet. They're still using relatively normal memory devices and having to construct them onto substrates to create "synthetic" wide band memory, simply because there's not enough demand worldwide to drive the manufacturing above 4,000-5,000 wafers a month. The memory guys will tell you that the minimum that they must have is 10,000 wafers a month to come down the learning curve, and they don't really want to touch anything that's less than 50,000 wafers a month. I think that's going to be a different trade-off and that may be an area, the SiP area, where we begin to see some expansion of some wafer-level packages.

**Andy Shaughnessy:** You speak at conferences and moderate panels, and you must hear a lot of questions. What are the big challenges that you're hearing about, especially from the design side?

**Bauer:** Well, I think that in the packaging arena, most of the challenges that I hear about are materials-related. There are some that are process related, and most of those in terms of uniformity, repeatability and consistency, those sorts of things. Warpage is an issue, especially in stacked 3D packaging. Most of those issues all come back to the materials, so there's a lot of interest in the materials. I will say that the problem is that nobody wants to pay anything more for the materials and that's always a paradox in the conflict between the materials suppliers and the manufacturers. Especially since the volume of material going into any particular package has reduced dramatically over the years, even as the number of packages has gone up. It's been a dichotomy for the material suppliers as well.

I think Happy is probably familiar with how long it has taken BCB (benzocyclobutene) to really become an established player, and BCB really came along in the 1980s as the substrate material for BGA packages. It's now starting to hold its own, but even today, when it comes down to price, people will go to FR-4 or FR-5 if they can. I think that that's the biggest challenge that I hear on a consistent basis—finding materials that'll do what you want them to do at a reasonable cost. And things like nano materials which I mentioned earlier. Nano materials are getting a lot of interest now, not necessarily for broad-based assembly, but certainly for assembly of high value-added components onto boards after it has been assembled and tested, and then they can put the high value component down after the fact.

**Shaughnessy:** We hear a lot of designers talk about how co-design is such an advantage. Do you see a lot of that going on?

**Bauer:** Happy and I have both been talking about that since the early 1980s. I remember the head of hybrid design at Tektronix when I first started, about 1984. He said hybrids wouldn't exist in 5-10 years because we'll be able to integrate it all into the silicon. I think we all know where that went. Whether you call it a hybrid or a multi-chip module or a system in package, we're still doing it.

---

**Whether you call it a hybrid  
or a multi-chip module  
or a system in package,  
we're still doing it.**

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I think the talk about co-design in most companies is just that. Unfortunately, there are two types of design that I would call design. One type refers to designing a product, where you have to incorporate all the manufacturing technologies together. The other type is the actual

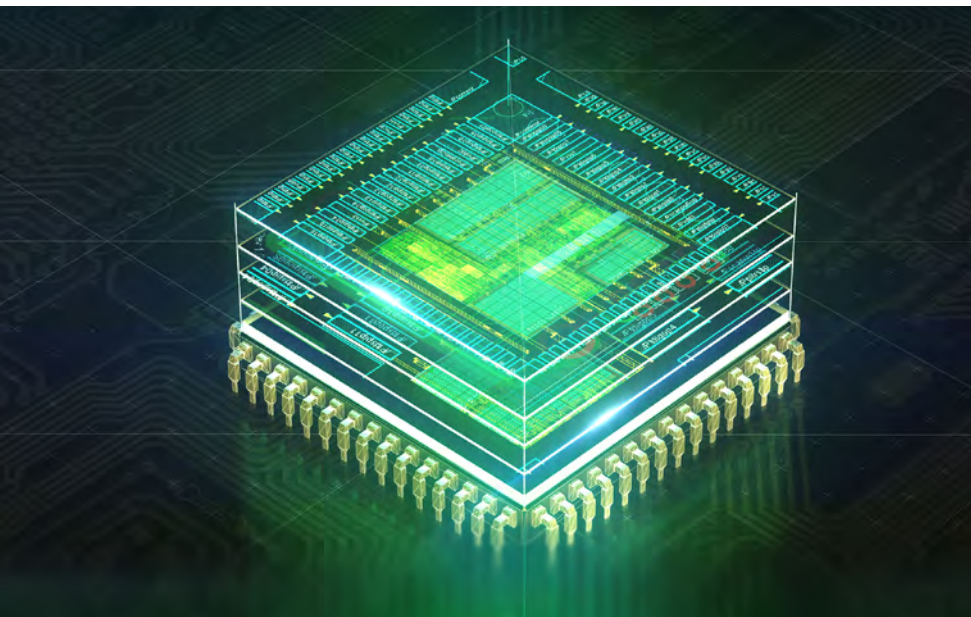


Figure 2: Packages have come along way over the past 60 years.

design of printed circuit boards, which in my mind is really not design—it's layout, because you're starting with the design. The circuit has been designed, the product has been architected, and now that layout designer has to figure out how to get all that hooked together within the confines of the space that has been allotted. Doesn't make the challenge any different, but it's a different kind of design. It's more of a problem-solving design as opposed to a creative design, not that there isn't any creativity in trying to solve the problem.

Those two different kinds of design present different perspectives. What I think you see is that if you could get a better interface between those two designers—the architect and the product designer who is trying to figure out how to build what he wants to build and then the layout designer who is trying to actually make sure that everything can and will go together—I think that's the conversation that we still lack.

We've done a lot of work, trying to get more feedback from manufacturing back to the product designer, and that has generated a lot of rules for the layout designer. The problem is that product designers just don't really listen well to the layout designer. Getting those two people to work together is very difficult; it's like getting the sales guy and the manufactur-

ing guy to agree on a delivery date!

**Barry Matties:** From an overall design rule practice, what do you think is the most important feedback from a fabricator or assembly facility?

**Bauer:** The interface between the printed circuit board fabricator and the printed circuit board designer is one place where the interface is actually fairly strong. Between them, they've been able to figure out what can and cannot be done. The layout designer and the fabricator tend to be close

enough together that they actually do a fairly decent job of that. It's not perfect, but they do a decent job.

When you make changes after the product has already been designed and put into production, it's another story. I think that when you talk about the fabricator or the assembly guy feeding back to the product designer, that's a much slower loop, for sure. The only time anybody gets any attention is when a product fails because the product designer screwed up, big time. Otherwise, it's the assembly house that ends up paying the piper by having to put in more effort to get the product out the door. Unfortunately, that tends to keep prices from coming down as fast as they might be able to if there was better communication on that side of the loop.

**Holden:** Chuck, is there a future for glass as an interposer instead of silicon? I spent the last three years working for Gentex. They process about 50 million square feet of glass a year. Extremely thin glass that's laser-cut and shaped and everything else.

**Bauer:** I think that glass is going to face the same issue that fan-out wafer-level packaging faces. Back in the years when I was at Tektro-nix, Corning Glass asked, "What can we do

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to facilitate the packaging industry?” We were looking at CerDIPs, ceramic dual in-line packages. I forget his last name, but Tom from Corning and I went out for dinner and talked about our volumes, and where they were going. He came back about six months later, and we talked again.

He said, “The problem is that at Corning, after looking at the market, we figured out that we could make enough glass for the entire worldwide CerDIP market in one of our laboratory batch ovens. We could make a 100-year supply in one batch.” The problem with glass as a substrate is, how does it capture any value? It’s such a low-cost material and the processing is where all the value-add is going to come in. It has a lot of potential, because it’s very stable. Not really that hard to work with, but just getting a good, solid supply chain in place is going to be extremely difficult.

**Matties:** Chuck, what practical advice would you give on packaging in general?

---

**If you ask an expert if something’s possible and he says yes, he’s probably right. If you ask an expert if something’s impossible, and he says yes, he’s probably wrong.”**

---

**Bauer:** If you ask an expert if something’s possible and he says yes, he’s probably right. If you ask an expert if something’s impossible, and he says yes, he’s probably wrong. I guess my advice would be that the most important two things that one needs to consider in looking at the future direction is, first, “is the approach or technology that you’re pursuing scalable?” Scalable can mean many things. One thing

obviously is if it is scalable to a manufacturing environment? More importantly, is your packaging technology scalable to the future of the circuit board and the chip? One of the big advantages that I saw in the GE embedded chip build up technology was that, because it relied on the same imaging metallization techniques that the chip guys were using, it would scale as the chips went to finer and finer geometries, and the package would can do that as well. So scalability is one thing.

The other thing is that if you’re looking at disruptive technology, you need to be able to see at least a 75% cost reduction within five years, or nobody’s going to talk to you because everybody knows that they can reduce the cost by 50% every two or three years just by continuing to beat on their suppliers, and become more efficient, more automated. Costs always are going down on the assembly side of things. Happy saw that and had to live with it when he was at Foxconn. So I would say to focus on scalability and on the cost impact of your technology.

**Matties:** Is there anything else you’d like to add?

**Bauer:** I would probably say that too many times, when we’re talking about technologies, whether we’re talking about wafer-level packaging or 3D packaging or whatever, we get too focused on the technology. We have to recognize that there are a lot of other risks besides the technical risk. There’s a market risk, there’s a financial risk, and you need to make sure that the market risk is minimized as well. You can’t disrupt the technology in a way that destroys your own market. I guess those would be the three points I would make.

**Matties:** Thanks, Chuck. We appreciate your time.

**Bauer:** All right. Thank you. **DESIGN007**



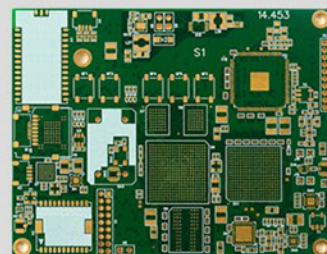
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# Standard PCB Component Families, Part 1

**Feature by Tom Hausherr**  
PCB LIBRARIES

Today, a wealth of PCB components and packages are available to the PCB designer and design engineer. Any senior designers who were laying out boards in the 1970s can remem-

ber when this was certainly not the case.

However, it can be difficult to wrap your head around the sheer number of components and packages on the market today. I hope this compendium of standard component families provides a handy resource for your next design.

## Standard Surface Mount Component Families

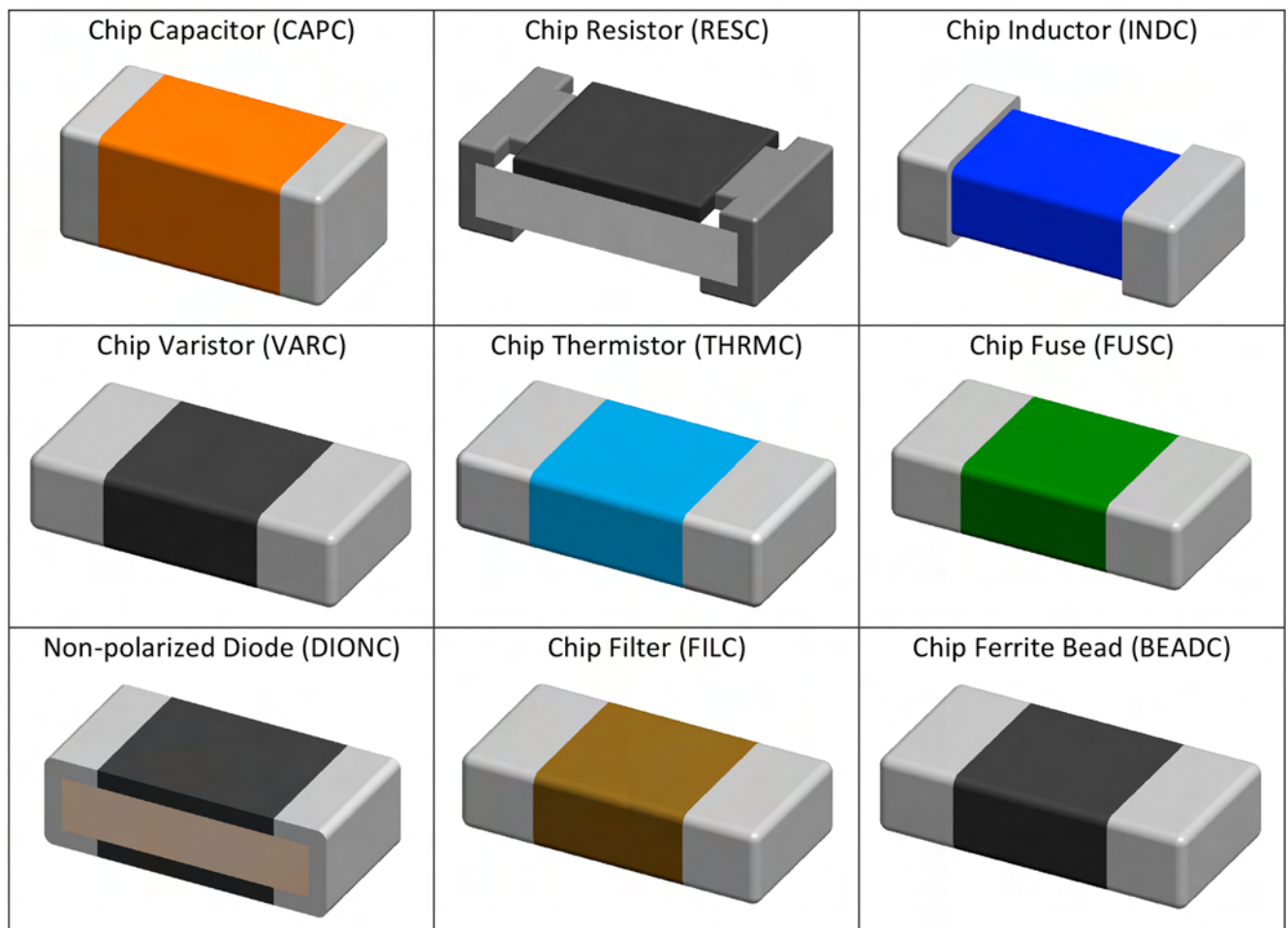


Figure 1: Non-polarized rectangular end-cap chip components.

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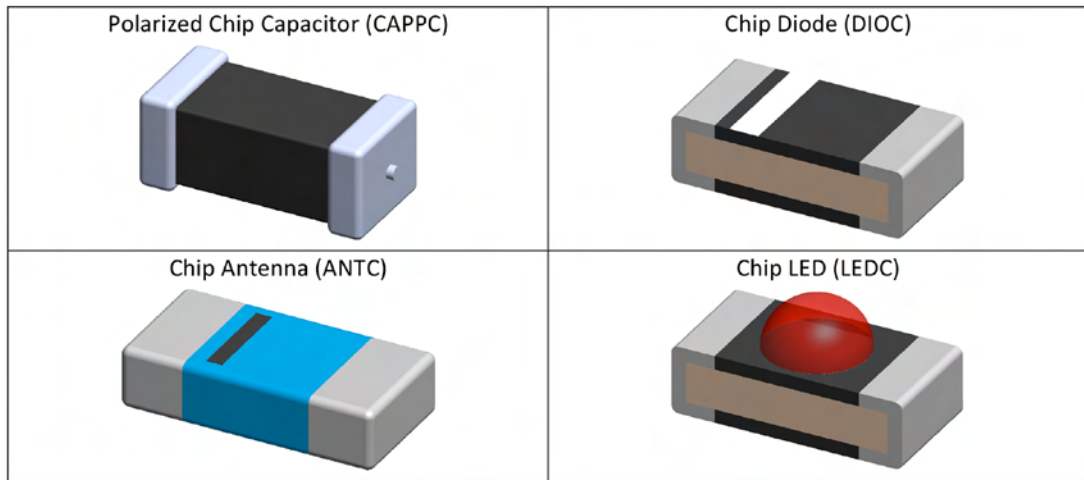


Figure 2: Polarized rectangle end-cap chip components.

Table of Chip Package Size Codes and Dimensions			
EIA (inch) Name	Inch Dimensions	IEC (metric) Name	Metric Dimensions
01005	0.0157 in × 0.0079 in	0402	0.4 mm × 0.2 mm
0201	0.024 in × 0.012 in	0603	0.6 mm × 0.3 mm
0402	0.039 in × 0.020 in	1005	1.0 mm × 0.5 mm
0603	0.063 in × 0.031 in	1608	1.6 mm × 0.8 mm
0805	0.079 in × 0.049 in	2012	2.0 mm × 1.25 mm
1008	0.098 in × 0.079 in	2520	2.5 mm × 2.0 mm
1206	0.126 in × 0.063 in	3216	3.2 mm × 1.6 mm
1210	0.126 in × 0.098 in	3225	3.2 mm × 2.5 mm
1806	0.177 in × 0.063 in	4516	4.5 mm × 1.6 mm
1812	0.18 in × 0.13 in	4532	4.5 mm × 3.2 mm
2010	0.197 in × 0.098 in	5025	5.0 mm × 2.5 mm
2512	0.25 in × 0.13 in	6332	6.4 mm × 3.2 mm
2920	0.29 in × 0.20 in	7451	7.4 mm × 5.1 mm

Table 1: Rectangular chip component package sizes.

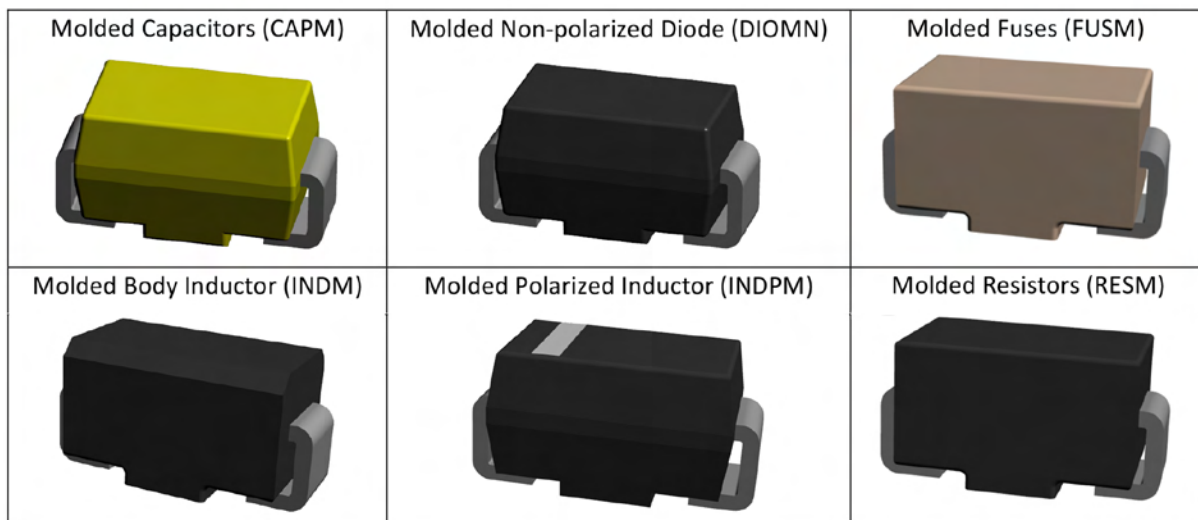


Figure 3: Non-polarized molded body inward flat ribbon components.

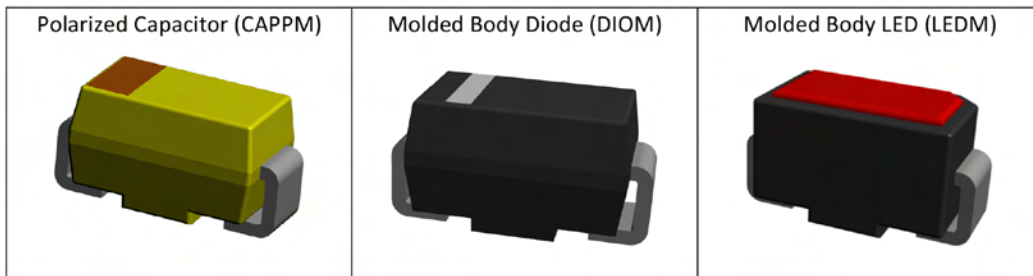


Figure 4: Polarized molded body inward flat ribbon components.

Common Molded Body Tantalum Capacitors			
EIA Size Code	Package Dimensions	KEMET Case Code	AVX Case Code
2012-12	2.0 mm × 1.3 mm × 1.2 mm	R	R
3216-10	3.2 mm × 1.6 mm × 1.0 mm	I	K
3216-12	3.2 mm × 1.6 mm × 1.2 mm	S	S
3216-18	3.2 mm × 1.6 mm × 1.8 mm	A	A
3528-12	3.5 mm × 2.8 mm × 1.2 mm	T	T
3528-21	3.5 mm × 2.8 mm × 2.1 mm	B	B
6032-15	6.0 mm × 3.2 mm × 1.5 mm	U	W
6032-28	6.0 mm × 3.2 mm × 2.8 mm	C	C
7260-38	7.3 mm × 6.0 mm × 3.8 mm	E	V
7343-20	7.3 mm × 4.3 mm × 2.0 mm	V	Y
7343-31	7.3 mm × 4.3 mm × 3.1 mm	D	D
7343-43	7.3 mm × 4.3 mm × 4.3 mm	X	E

Common Molded Body Diodes		
JEDEC Standard	Case Code	Package Dimensions
DO-214AA	SMB	5.30 mm × 3.60 mm × 2.25 mm
DO-214AB	SMC	7.95 mm × 5.90 mm × 2.25 mm
DO-214AC	SMA	5.20 mm × 2.60 mm × 2.15 mm

Table 2: Some common molded body tantalum capacitors and diodes.

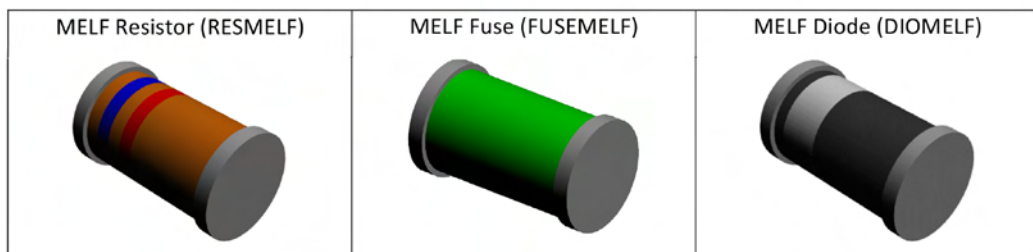


Figure 5: Metal electrode leadless face (MELF).

Common MELF Package Sizes		
Common Case Names	Size Code	Package Dimensions
MicroMelf (MMU)	0102	2.20 mm L X 1.10 mm Dia.
MiniMelf (MMA)	0204	3.60 mm L X 1.40 mm Dia.
Melf (MMB)	0207	5.80 mm L X 2.20 mm Dia.

Table 3: Some common MELF package sizes.

Small Outline Diode (SOD)

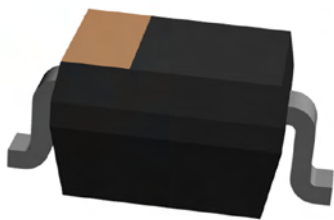


Figure 6: Small outline diode (SOD) with gull-wing leads.

Small Outline Diode Flat Lead (SODFL)

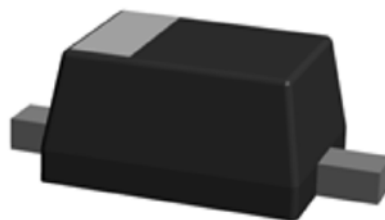
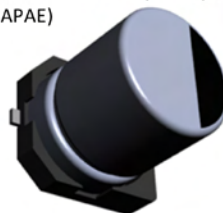


Figure 7: Small outline diode flat lead (SODFL).

Common Small Outline Diode (SOD) Sizes	
Case Code	Package Dimensions
SOD-123	3.68 mm × 1.17 mm × 1.60 mm
SOD-128	5.00 mm × 2.70 mm × 1.10 mm
SOD-323	1.70 mm × 1.25 mm × 0.95 mm
SOD-523	1.25 mm × 0.85 mm × 0.65 mm
SOD-723	1.40 mm × 0.60 mm × 0.59 mm

Table 4: Some common small outline diode sizes.

Aluminum Electrolytic Capacitor (CAPAE)



Crystal (XTAL)



Figure 8: Under body L-bend lead (CAPAE & XTAL).

Side Concave Crystal (XTALSC)



Side Concave Inductor (INDSC)

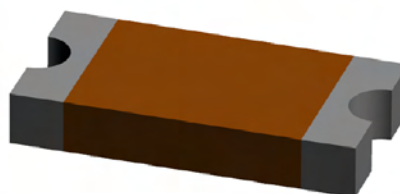


Figure 9: Non-polarized side concave packages 2-pin.

Side Concave Diode (DIOSC)



Side Concave LED (LEDSC)

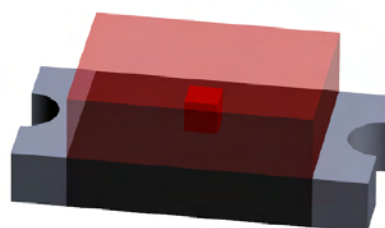


Figure 10: Polarized side concave packages 2-pin.

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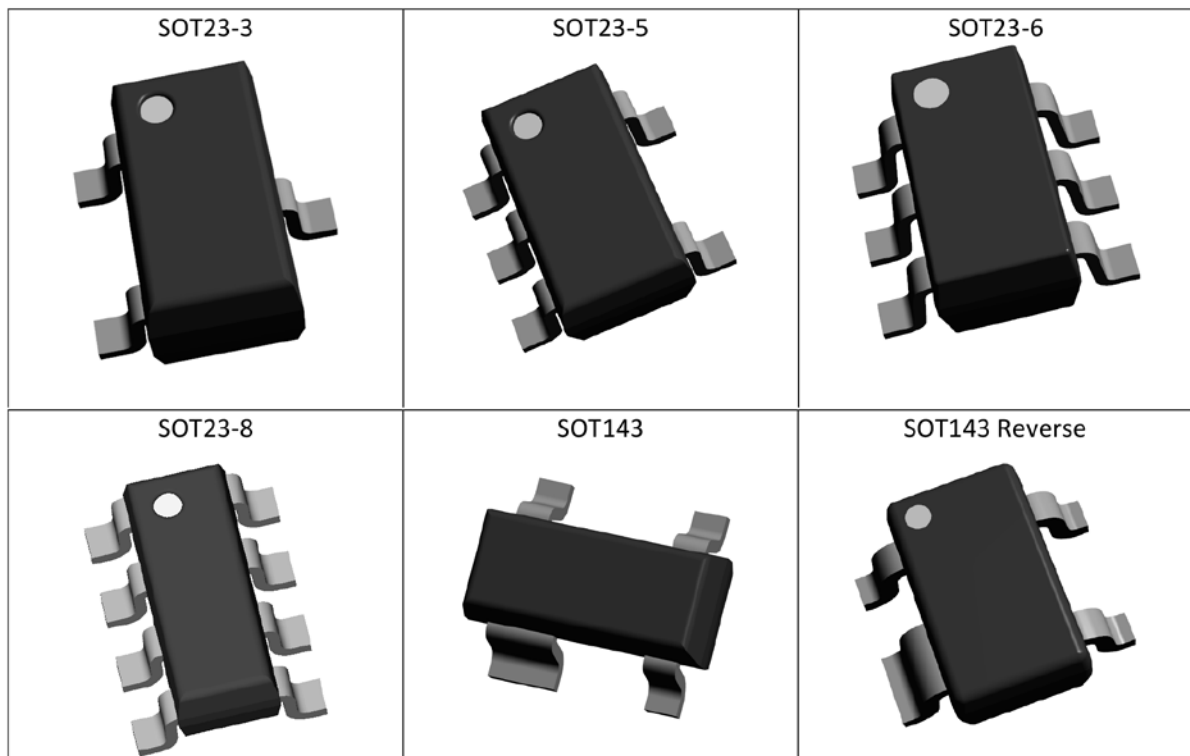


Figure 11: Small outline transistor SOT23 & SOT143 (SOT).

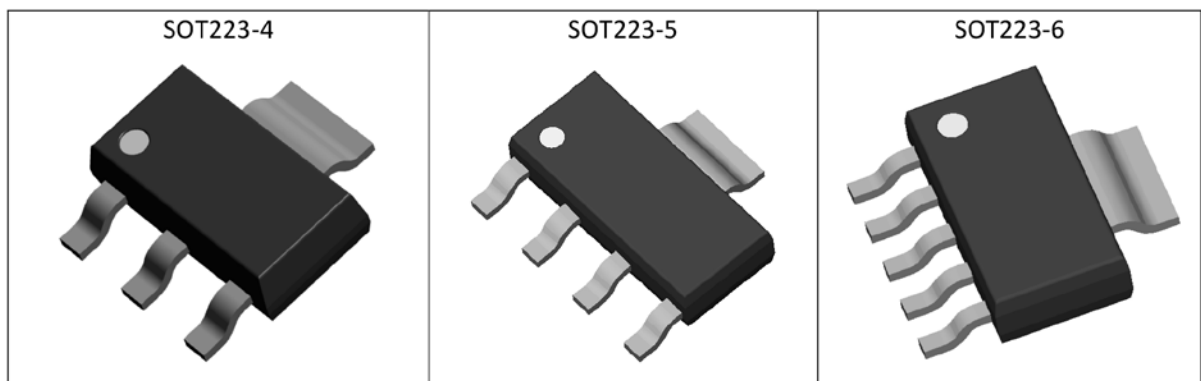


Figure 12: Small outline transistor SOT223 (SOT).

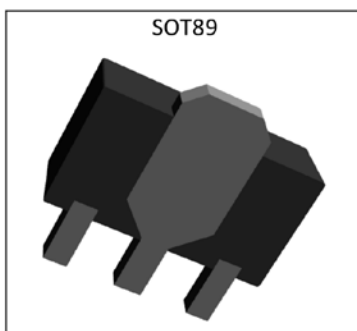


Figure 13: Small outline transistor SOT89 (SOT).

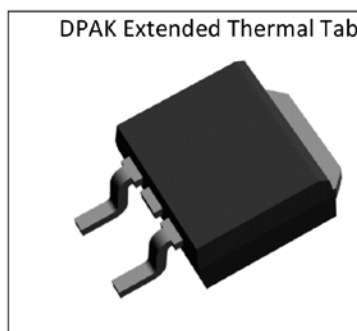


Figure 14: DPAK.

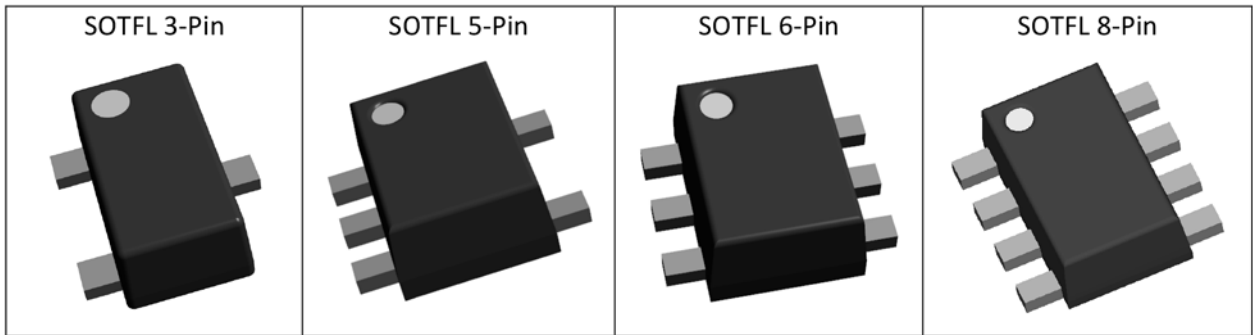


Figure 15: Small outline flat lead transistor (SOFL).

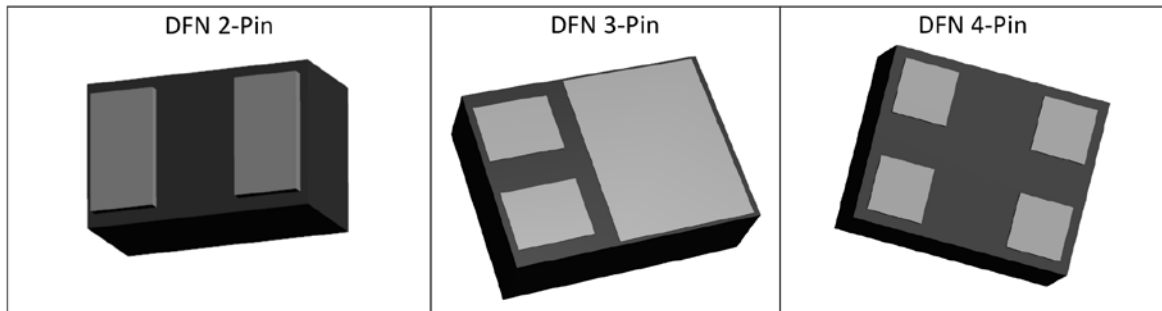


Figure 16: Diode, resistor, inductor, capacitor, crystal, fuse, transistor, dual flat no-lead (DFN).

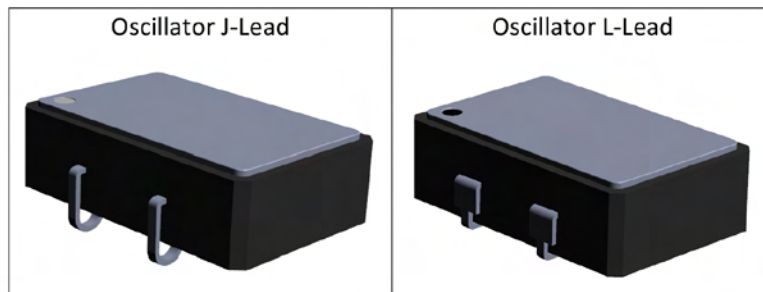


Figure 17: J & L-lead oscillators (OSC).



Figure 18: Oscillator, side & corner concave (OSCSC).

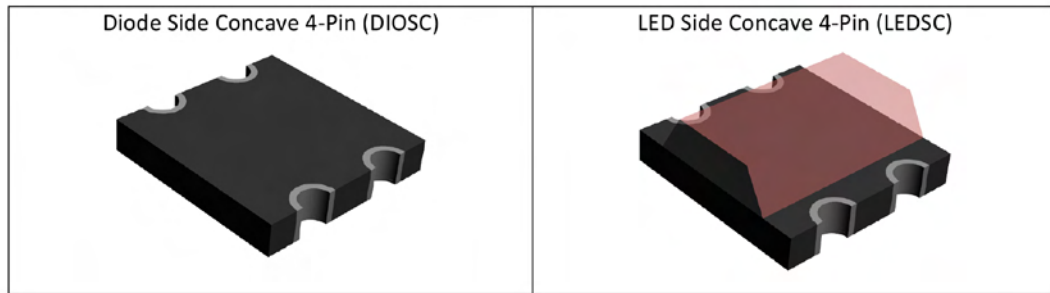


Figure 19: Side concave (4-Pin) diode and LED.

All 3D package models in this article were auto-generated by the free Library Expert Pro using package dimensions provided by the component manufacturer datasheet.

Part 2 of this feature will be published in the September issue of *Design007 Magazine*, and the collection will be made available online in its entirety. **DESIGN007**



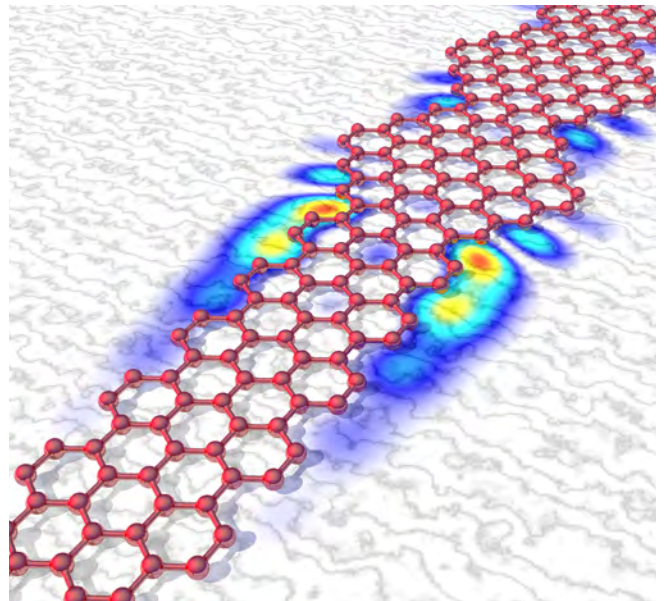
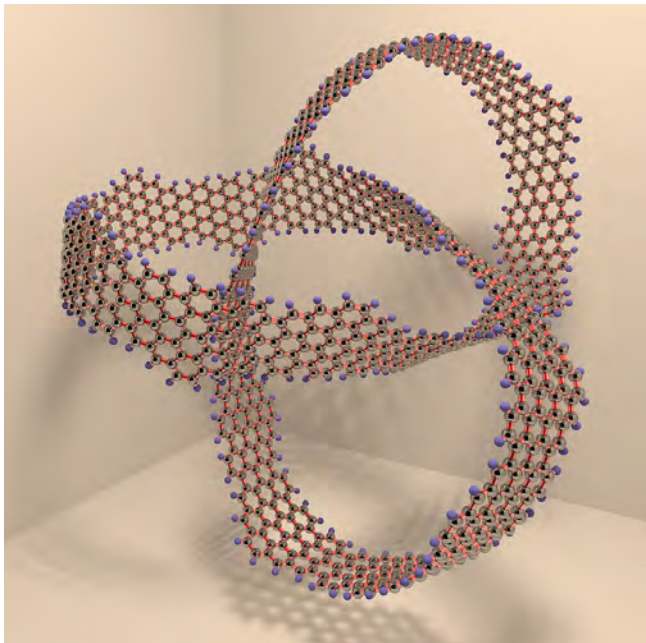
**Tom Hausherr CID+, CIT**, is president of PCB Libraries.

## Quantum Chains in Graphene Nanoribbons

Empa researchers and colleagues from the Max Planck Institute for Polymer Research in Mainz and other partners, have achieved a breakthrough to be used for precise nanotransistors or possibly even quantum computers, as the team reports in the current issue of the scientific journal *Nature*.

A material that consists of atoms of a single element but has completely different properties depending on the atomic arrangement. The graphene ribbons, which are only a few carbon atoms wide and exactly one atom thick, have very different electronic properties depending on their shape and width: conductor, semiconductor or insulator.

Source: Empa





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work smarter  
not harder

## PCB Design Challenges: A Package Designer's Perspective

**Feature by Bill Acito**  
CADENCE DESIGN SYSTEMS

The challenges faced by the PCB designers of today are significant. If we examine the breadth of designs, we find ever-increasing data rates and more high-speed signal routing that drive additional challenges meeting signal-quality requirements, including reflection signal loss and crosstalk issues. At the same time, designers are being asked to complete designs in shorter cycle times and in smaller form factors. They must come up with new and more complex routing strategies to better control impedance and crosstalk. Manual implementation is often time-consuming and prone to layout errors. Designers have an increased need for pre-layout simulation to evaluate the design early on and establish routing strategies.

Designers are faced with conflicting requirements. The PCB designer is expected to do more with less space. The overall density of designs is increasing. Balanced against cost constraints, the PCB designer may leverage

high-density interconnect (HDI) technology to compress the design into the available space, which in turn increases the likelihood of signal integrity issues. Cost pressures may force the PCB designer to reduce layer count or, at the very least, stay within the layer count that has been budgeted.

The PCB designer finds himself in a constant battle to converge on a design that meets all the design constraints. EDA vendors have provided a suite of various tools and automation to assist with the manufacturing constraints and physical and signal integrity physics of the design—breakout tools, route feasibility and estimation, timing and delay match, HDI-compliant design, and flex and embedded component design. Without a doubt, the challenges are significant for the PCB designer. If the constraints cannot be surmounted with technology, perhaps the solution is to work smarter.

So, rather than looking at some of the advanced additive technologies and other PCB manufacturing capabilities that could enable us to work at a significantly finer pitch, albeit

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###### Rigid Flex Technology

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##### QUANTITIES

From Prototypes to Full Scale Production Orders

at a higher cost, let's focus on those capabilities that allow us to work smarter. As an IC packaging EDA engineer, I argue that working collaboratively with the system design and packaging engineers is one way we can enable denser designs that are completed faster, while still meeting signal integrity and power integrity requirements. Doing so requires more pre-planning and pre-analysis of the design, specifically looking at breakout patterns from the high pin-count devices, the critical signal typologies and routing schemes, and an up-front analysis of the critical signals within the design.

Due to the complexity of designs and increased time pressures, the PCB designer may reap significant rewards by spending time planning the PCB design within the context of the components that will be mounted on the board. Spending more time on the initial planning and partitioning of the design intercon-

nect could allow the PCB designer to keep the number of layers low and meet the intended form factor and cost targets. How is this possible?

## Cross-Domain Planning

The PCB designer's ability to not only work within their own domain, but also extend their influence into the domain of the package designer, allows them to enlarge the available solution space. In many cases, large BGA footprints are no longer fixed entities but footprints that can be modified and optimized to assist the PCB designer in the completion of the task, as shown in Figure 1.

Where possible, the PCB designer should have a mechanism to plan and optimize the entire system at a high level of abstraction before parts are placed on the board. Where there are large BGA footprints that are not fixed and still under design, they must have the abil-

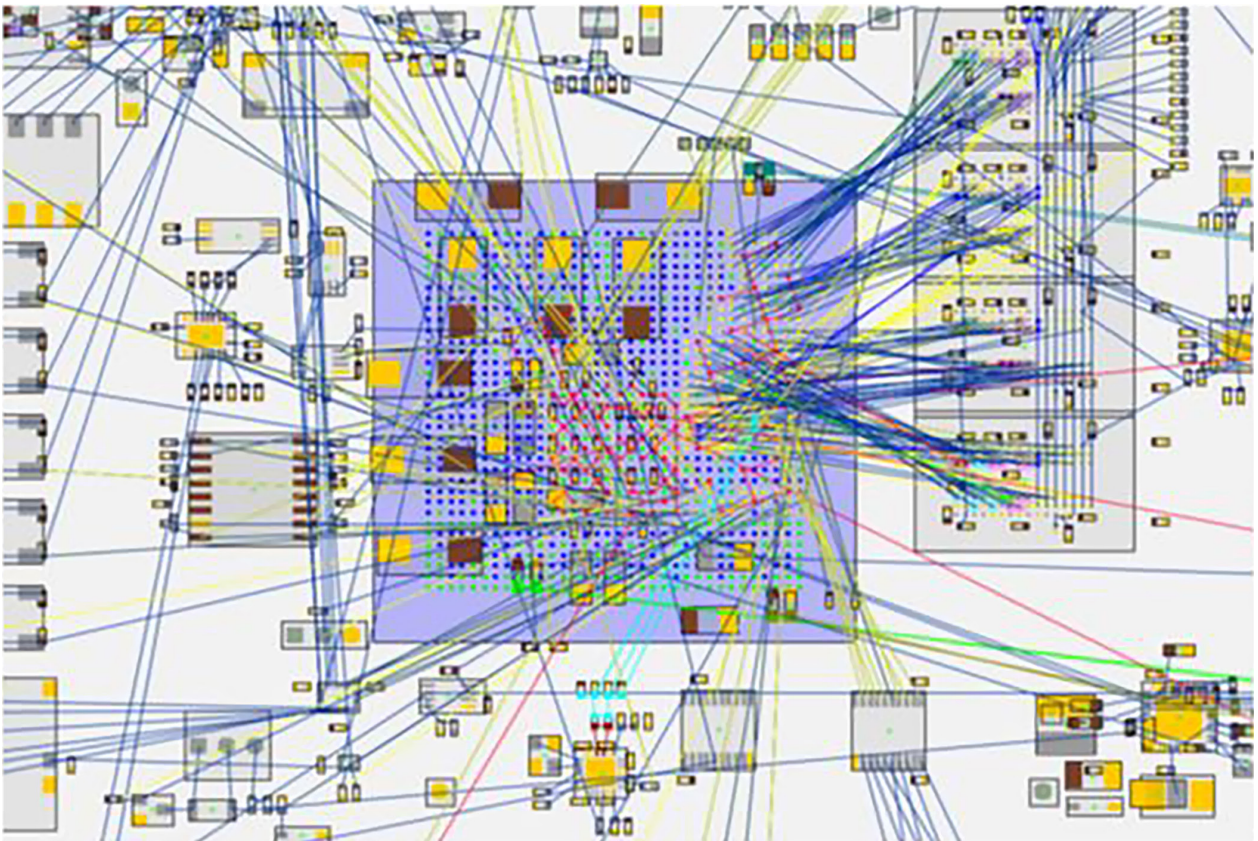
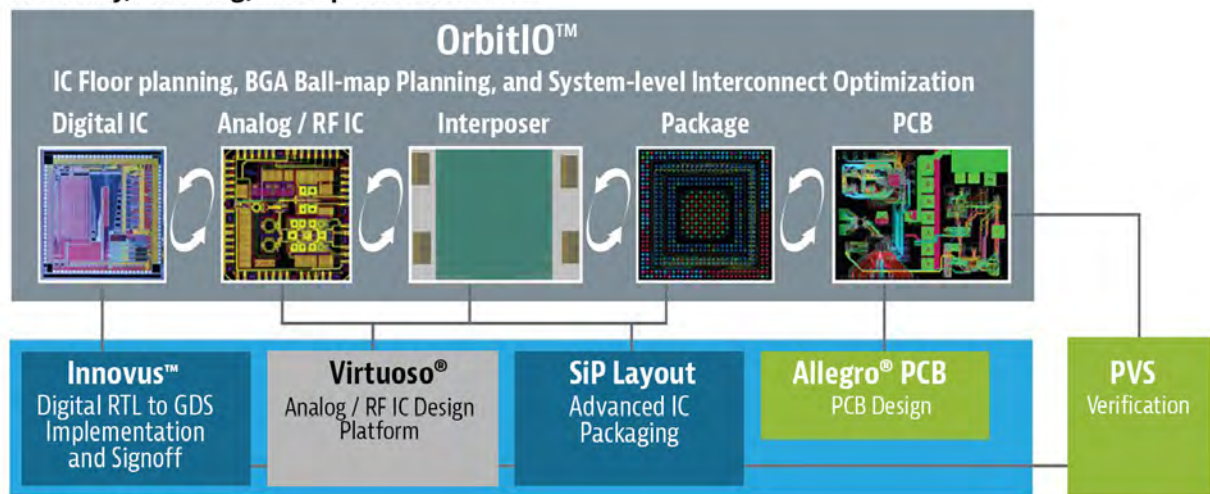


Figure 1: Board-driven ball map optimization.

## Assembly, Planning, and Optimization Level



## Implementation Level

Figure 2: Cross-domain planning.

ity to access and modify those packages. Given that access, not only can the PCB designer evaluate the impact of component placement on the routability and layer count, but they have the ability to suggest modifications to the larger components to optimize their breakout and power access and minimize layer count.

Providing a tool that allows the PCB designer to see the physical extents of the board as well as the packages, and to look at the interconnect organized by the critical buses, gives the user the ability to optimize placement and assignment to meet these goals (Figure 2). At this stage of the design process, the PCB designer

does not need all the constraints or detailed routing; they can work at a level of abstraction that allows them to partition the design and assess the interconnect in a simplified state.

In vertical design environments where the organization not only owns the design of the PCB but also the critical device packages (and the IC), all the design domains can be brought into play and optimized. A single common view can be provided as a design environment to the user and can support the hierarchy of the entire system, including backplanes, daughter-cards, packages, interposers, and even the die I/O ring.

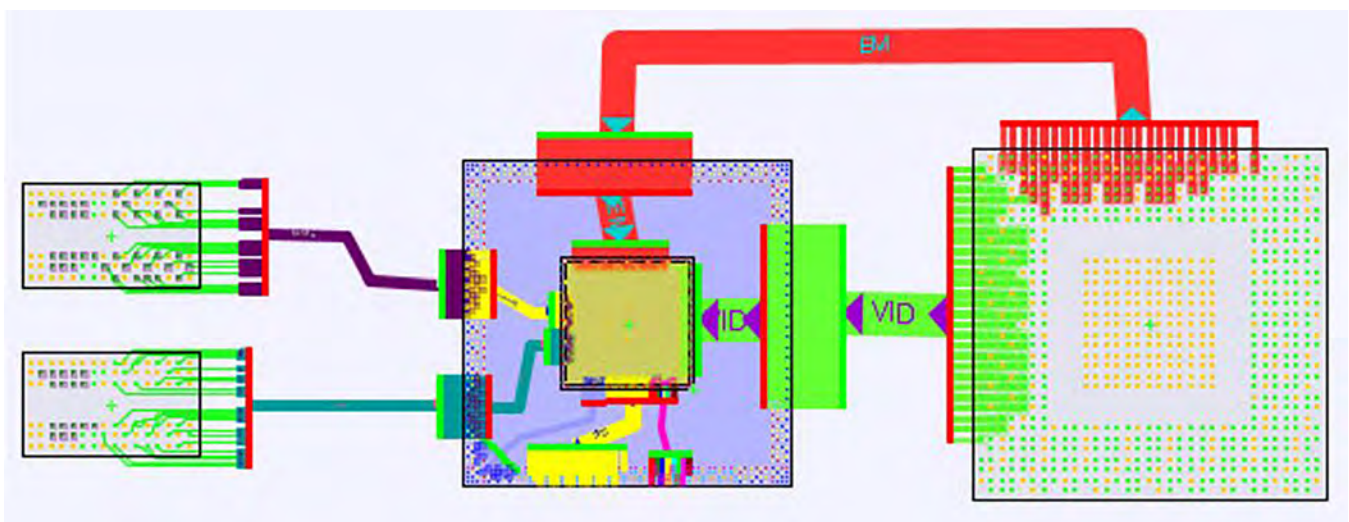


Figure 3: Interconnect flow planning.

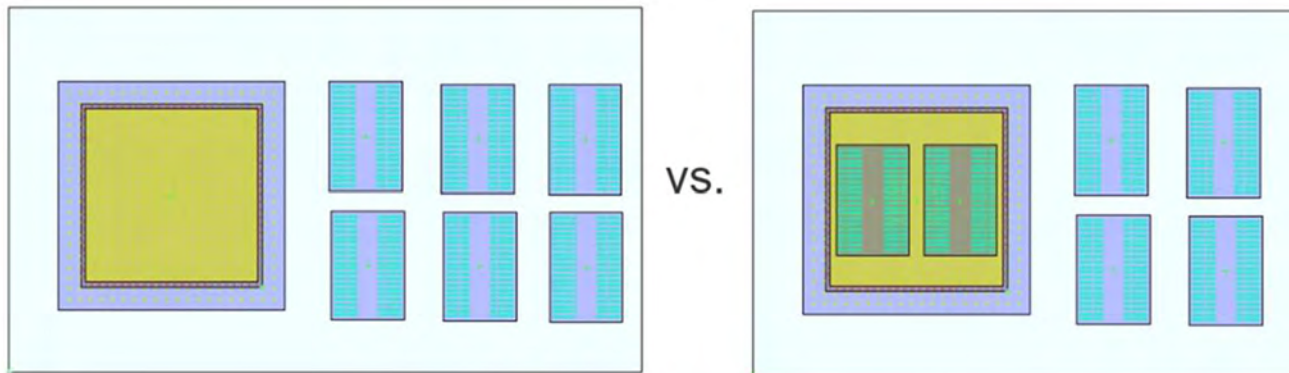


Figure 4: Hierarchy options.

The design environment can allow the user to assign, group, plan, and connect the various interfaces of the system. Data buses can be represented and treated as one path entity, and once the route has been planned, the user can manipulate the routing escape breakout and channels and modify the escape sequencing and assignment to create the interconnect in as few layers as possible, possibly in one (Figure 3). The system designer can also use this capability to look at various versions of partitioning and organization—should the CPU connect to the memory on the PCB, or should the connectivity be integrated into the package or an interposer (Figure 4)?

With 2.5 and 3D integration in the package, system planners now have additional integration vehicles available to help save space and meet high-speed signal bus constraints. Those designs that require a CPU working with a high-density memory like high-bandwidth memory (HBM) can take advantage of the close proximity and tighter integration that can be achieved in an IC package or an interposer rather than a PCB. Advanced packaging technologies are now one more vehicle allowing the system designer to implement in a smaller form factor; having a cross-domain system planning tool that can manage the design in the PCB and packaging space is an advantage.

Once the overall design is planned at a high level of abstraction, the system design can then be transferred over to the implementation tools. Depending on the design's complexity, it may spawn one or many databases including

not only the PCB design, but also the package design, possibly an interposer, or the design of the integrated circuit itself. The system design team moves from a higher level of abstraction to the more detailed substrate and board implementations. Here, the detailed routing and manufacturing constraints can be applied, and a more precise level of co-design can be leveraged.

## Co-Design

The updates and engineering change orders (ECOs) in the design certainly do not stop at the initial planning phase. The ability to continue to make changes and updates as the design implementation is completed is a necessary capability as implementation and more detailed analysis exposes additional issues.

In the implementation phase, the PCB designer must focus on escape routing, working within the maximum layer count while also meeting the signal and power integrity requirements of the design. At this stage, we are applying very specific routing technologies to meet the signal integrity and power integrity requirements of the system. The PCB designer may have no option other than to work with the packaging engineer to swap assignments or optimize the interconnect to meet these goals.

This concept of co-design is not new or unique. For years, designers have been using various techniques to plan and co-design between IC packages and the PCB. Spreadsheets are often used to define and manage footprints in the design. However, even a

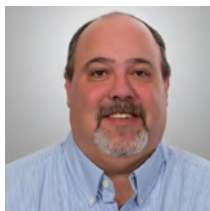
spreadsheet can be difficult to work with and error prone. This is an opportunity for data to be lost, misrepresented (e.g., “What is the orientation of the BGA footprint?”) or accidentally modified.

Throughout the process of pathfinding and co-design between the package and the PCB, the PCB designer needs the ability to evaluate the layout at each level of detail. Providing a mechanism to evaluate the design, even at the higher level of abstraction of the system, ensures that the PCB designer does not make layout mistakes early in the process. Those mistakes could eventually cause PCB designer to modify the design late in the overall design process with significant effort and delay.

Likewise, having a mechanism to provide signal integrity feedback to the PCB designer as they work on the layout can significantly shorten the design time. As the design progresses and the design team transitions to implementation, the level of analysis can increase and eventually converge on a design that meets both physical and electrical requirements with the least amount of iterations.

## Summary

Density, time and performance requirements are intensifying and in conflict. Short of significant innovations in PCB manufacturing, design teams must work much smarter and more efficiently to meet their design goals. Planning the design up front and leveraging the packaging design domain in the overall design is another tool that the PCB designer can use to meet their goals. **DESIGN007**



**Bill Acito** is an IC packaging product engineer for Cadence Design Systems in Chelmsford, Massachusetts.

# Quick Memory

Computer memory capacity has expanded greatly, allowing machines to access data and perform tasks very quickly, but accessing the computer's central processing unit, or CPU, for each task slows the machine and negates the gains.

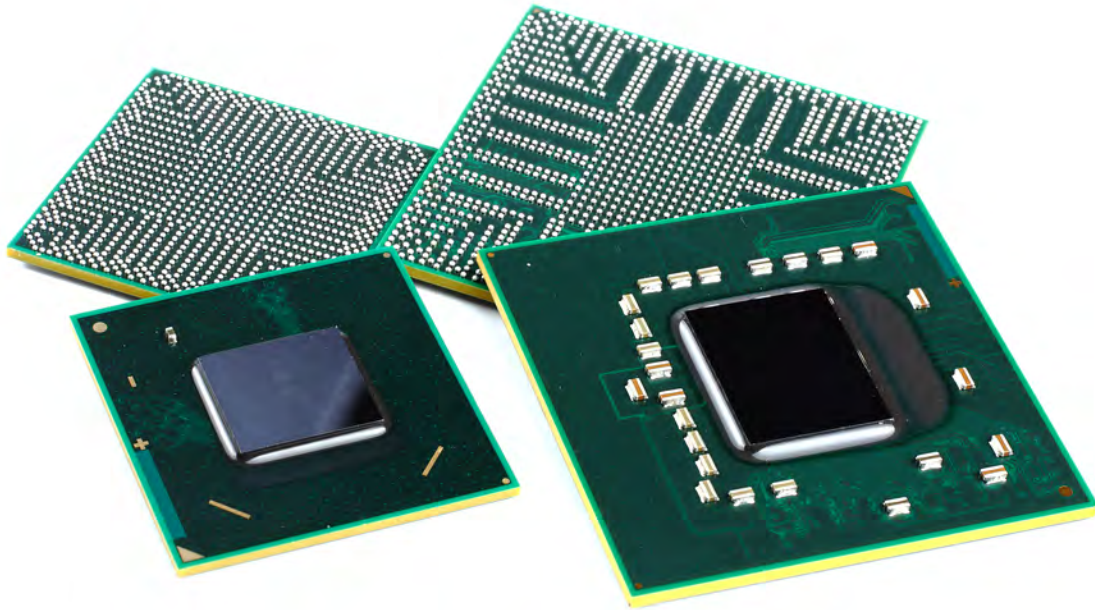
To counteract this issue, known as a memory wall, computers use a cache, or hardware component that stores recently accessed data that has already been accessed so that it can be accessed faster in the future. Song Jiang, an associate professor in the Department of Computer Science and Engineering at The University of Texas at Arlington, is using a three-year, \$345,000 grant from the National Science Foundation to explore how to make better use of the cache by allowing programmers to directly access it in software.

“Efficient use of a software-defined cache allows quick access to data along with large memory. With memory becoming more expansive, we need to involve programmers to make it more efficient. The programmer knows best how to use the cache for a particular application, so they can add efficiency without making the cache a burden,” Jiang said.

When a computer accesses its memory, it must go through the index of all the data stored there, and it must do so each time it goes back to the memory. Each step slows the process. With a software-defined cache, the computer can combine or skip steps to access the data it needs automatically without having to go through the memory from the beginning each time.

Source: Univ. of Texas Arlington





# BGA Fanout Routing Overview

**Feature by Christian Keller**  
 ALTIUM

PCB developers are deluged with new challenges caused by increasing density and smaller components. Ball grid arrays (BGAs) create particular challenges during layout, with hundreds of connections in just a few square centimeters. Fortunately, designers now have options for addressing these issues.

## Fanout and Escape Routing

Because of the density and distance from the connection points, only the two outermost rows of a BGA can be connected directly to surface circuit traces. All other terminals of the BGA cannot be connected in a direct path on the surface.

Fanout and escape routing is integrated in many PCB design systems to enable further connections. In fanout and escape routing, the two outermost rows, and all other rows of a BGA, are automatically connected to the center of the terminals via a short circuit trace that is executed at a 45° angle. This provides a

blind via that forms a direct connection to the next signal layer. Routing can be executed on the next signal layer.

Using via-in-pad eliminates the need for the additional trace to the center of the connections, thereby creating additional space for circuit traces. Therefore, with via-in-pad, the through contact can be placed directly at the terminal of the BGA.

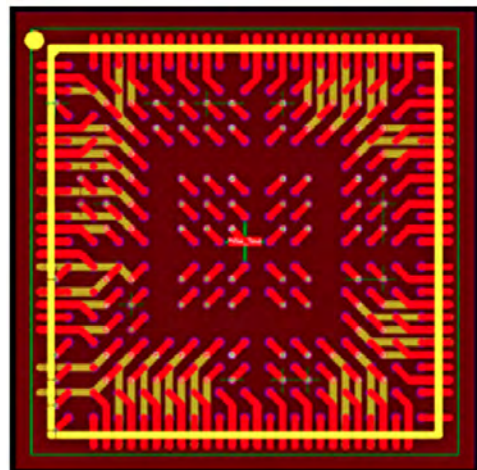


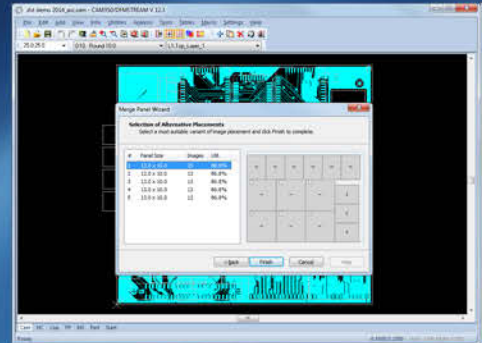
Figure 1: BGA with classic fanout routing of all the electrical connections.

# Solutions to Ensure PCB Manufacturing Success!



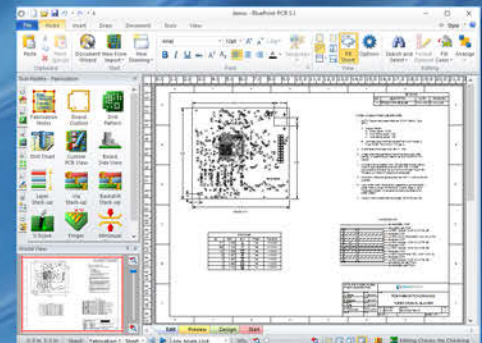
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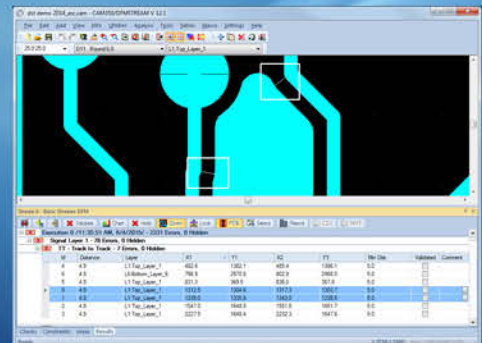
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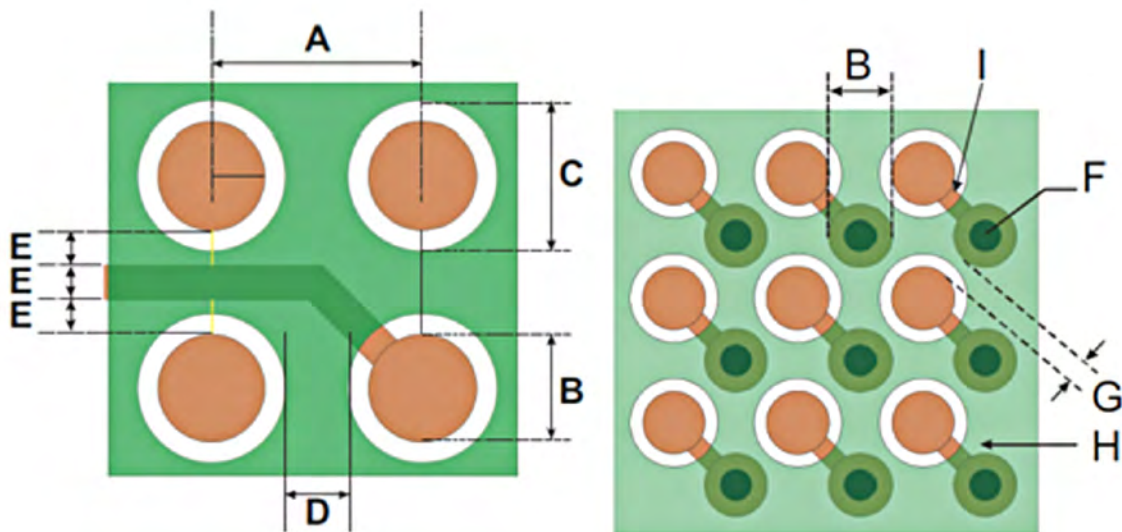


Figure 2: Visual representation of terminals of a BGA with their connection possibilities.

During circuit board manufacturing, these through contacts will be filled with a non-conducting medium and cured. Later, the ends are metallized, planarized, and also over-contacted. This makes the surface of the via flat and can be used as the contacts of the BGA. This solution can be used for both stacked and staggered microvias and/or blind vias. IPC-4761 describes how via-in-pads, for example filled and capped vias (IPC-4761 Type VII), are prepared. Despite the higher manufacturing costs, via in pads will always be preferred, because of the higher integration density of

BGAs and their lower inductance at high frequencies (signal quality).

Fanout routing features in today's tools let you decide between the classical fanout (auto or BGA) and via in pad. For classic fanout routing, Altium Designer offers all the necessary settings for the direction of the fanout (direction from pad) whether the via should be placed in the center between the terminals of the BGA or not (via placement mode). The via is placed between the terminals of a BGA in most cases, because of costs and ease of manufacturing.

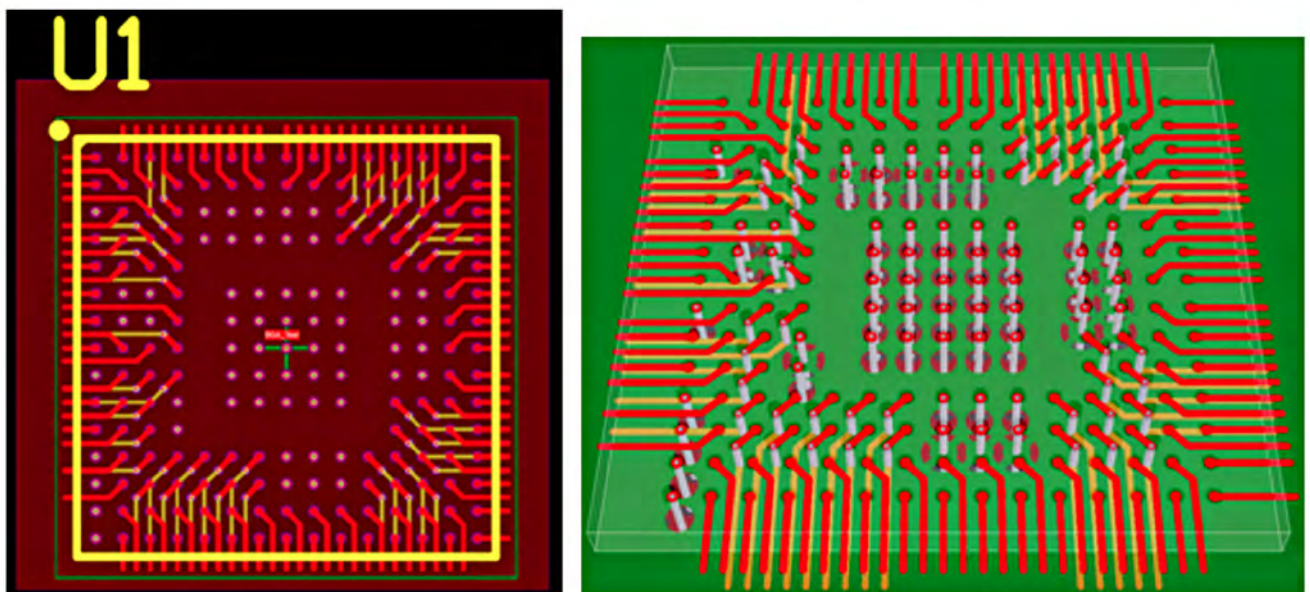


Figure 3: Signal lead with fanout and escape routing and a voltage supply connection as with via-in-pad.

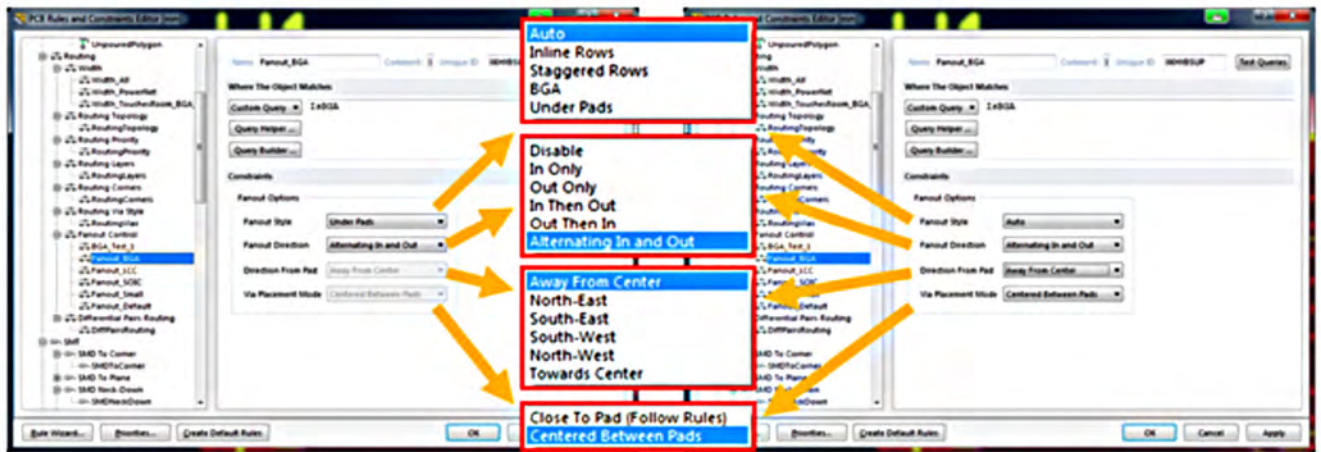


Figure 4: Design rule editor (fanout control) in Altium Designer.

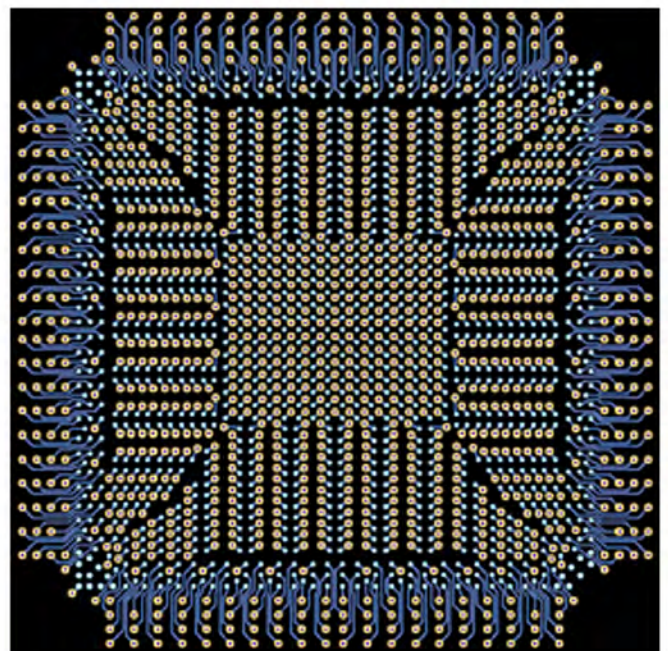
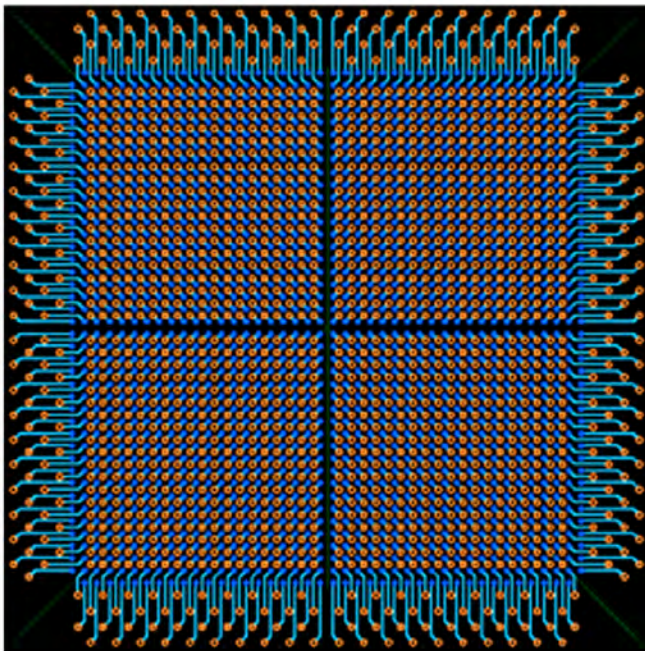


Figure 5: Different pin assignments for the fanout and escape routing of BGAs.

In many cases, the via is shifted toward the terminals. Escape routing is optimized with this “off-grid” connection. However, a new strategy for fanout and escape routing must be defined for each BGA. The classical autorouter available in most ECAD systems quickly runs into its limitations.

PCB manufacturing has improved to accommodate the finer features needed to break out BGAs. Dimensions of trace width and minimum via size have all shrunk. High-density interconnect (HDI) has also become more and

more common for high-speed boards with very dense parts placement.

A pad size of .018” (0.45 mm) and a drill diameter of .006” (0.15 mm) are considered a standard for through-hole connections for 1 oz. copper. Contact your PCB fabricator to determine their exact minimums for these and other manufacturing-critical dimensions.

When working with BGA breakouts, narrower traces can be used near the device to facilitate getting the signals out from the package. However, it’s virtually impossible to maintain target

impedance with traces less than .004" on common substrates. Because of that, these traces should only be used near the device for breakout and not generally across the entire PCB.

## Summary

PCB designers have become used to ever-shrinking boards and components, trends that will continue for the foreseeable future. New technologies, such as via-in-pad, smaller traces near BGAs, and design rules incorporated into

today's modern EDA tools can give designers the tools to layout these signal-dense devices. Using these tools can make breaking out and routing BGAs as painless as is possible. **DESIGN007**



**Christian Keller** is a field applications engineer with Altium.

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# New 3D-Printed Device Could Help Treat Spinal Cord Injuries

Engineers and medical researchers at the University of Minnesota have teamed up to create a groundbreaking 3D-printed device that could someday help patients with long-term spinal cord injuries regain some function.

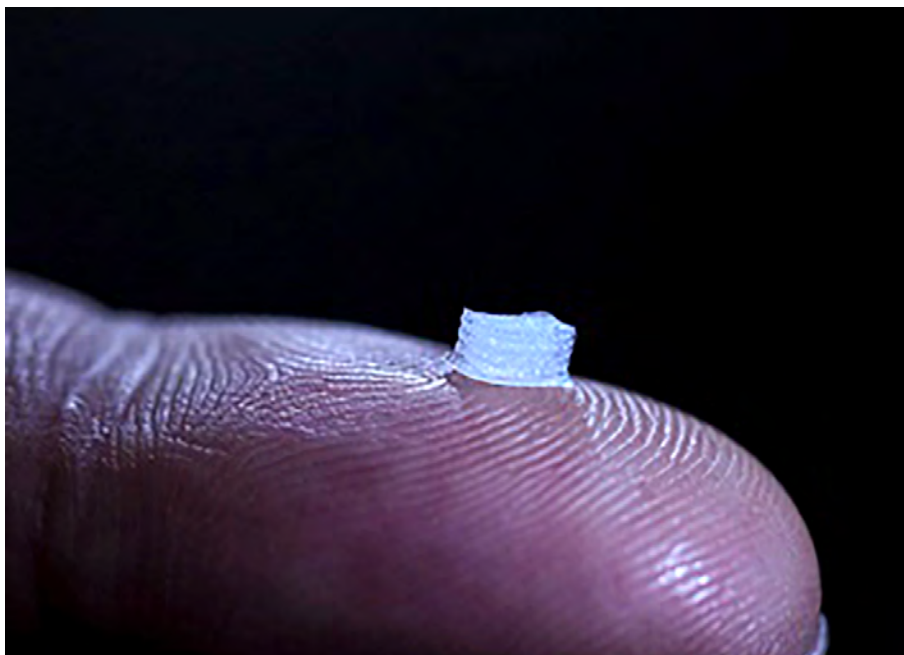
A 3D-printed guide, made of silicone, serves as a platform for specialized cells that are then 3D printed on top of it. The guide would be surgically implanted into the injured area of the spinal cord where it would serve as a type of "bridge" between living nerve cells above and below the area of injury. The hope is that this would help patients alleviate pain as well as regain some functions like control of muscles, bowel and bladder.

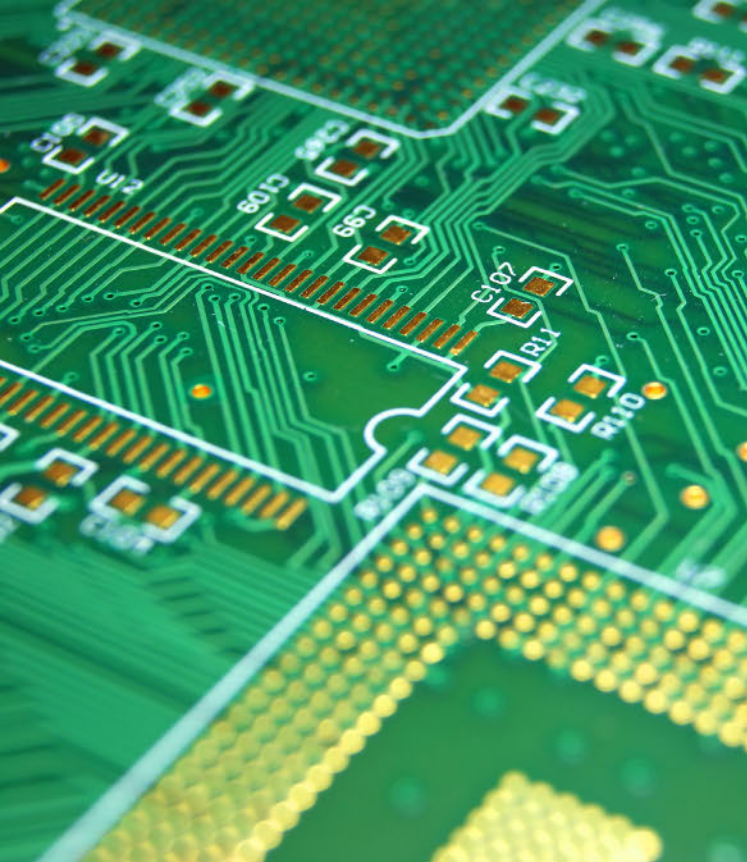
"This is the first time anyone has been able to directly 3D print neuronal stem cells derived from adult human cells on a 3D-printed guide and have the cells differentiate into active nerve cells in the lab," said Michael McAlpine, Ph.D., a co-author of the study and University of Minnesota Benjamin Mayhugh associate professor of Mechanical Engineering in the University's College of Science and Engineering.

"This is a very exciting first step in developing a treatment to help people with spinal cord injuries," said Ann Parr, M.D., Ph.D., a co-author of the study and University of Minnesota Medical School assistant professor in the Department of Neurosurgery and Stem Cell Institute. "Currently, there aren't any good, precise treatments for those with long-term spinal cord injuries. Everything came together at the right time. We were able to use the latest cell bioengineering techniques developed in just the last few years and combine that with cutting-edge 3D-printing techniques."

There are currently about 285,000 people in the United States who suffer from spinal cord injuries, with about 17,000 new spinal cord injuries nationwide each year.

Source: Univ. of Minnesota





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# PCB007 Highlights



## EIPC 50th Anniversary Conference Day 1: The Past, the Present and the Future, Pt. 1 ▶

Just like old times—meeting with John Ling, with whom I had previously travelled to industry events for over two decades, and who still carries the role of EIPC marketing manager, to fly together from Birmingham UK to Dusseldorf in Germany for the EIPC 50th Anniversary Summer Conference.

## EIPC 50th Anniversary Conference Day 2: The Past, the Present and the Future, Pt. 1 ▶

The sun was shining in Dusseldorf as delegates returned to the conference room for the second day of the EIPC 50th Anniversary Conference. There were very few empty chairs as Paul Waldner opened the proceedings with Session 5, on a theme of future PCB design, material, and processes for the PCB supply chain.

## Graphic Plc Continues to Prosper at 50 ▶

Graphic Plc was formed on 21st June 1968 by Rex Rozario OBE. Rex worked with Dr Paul Eisler, the inventor of the Printed Circuit Board, at Technograph-Telegraph in the 1950s. In 1972 Rex moved the factory to Crediton and operated from a number of buildings on the Lords Meadow Industrial Estate.

## The Right Approach: The Value of Coopetition ▶

As our industry continues to evolve and shape-shift, PCB manufacturing continues to shrink through consolidations and attrition. In a global economy, partnering with world-class suppliers is mandatory, and excluding a subset of this dwindling supply base because they also happen to be in a crossover business will severely hinder this effort.

## Punching Out! Dealing with Family Businesses ▶

Some families may have spent this past Father's Day discussing family business issues, including when, how or whether to pass the baton. There are several issues to consider when dealing with a family business.

## Flex Time: Why is Rigid-Flex So Expensive? ▶

Why is rigid-flex so expensive? In this article I'll share with designers the cost drivers in rigid-flex relative to standard rigid boards and flex circuits with stiffeners.

## RMAs: Negative Experience or Valuable Opportunity? ▶

Non-conforming material that is sent back by the customer can easily be interpreted as a negative experience. However, if it is perceived as an opportunity to learn and support the customer it becomes a much more pleasant and satisfying endeavor.

## It's Only Common Sense: Love What You Sell ▶

Raise the perceived value so high that our customers will feel guilty even haggling about the price. To do this, you must love your products—love them as much as my dad, the Coke man, loved his.

## PCB Material Toolbox for Today's 3G and 4G Networks and Future High-Speed Needs in 5G ▶

The material toolbox idea first came up when I saw the IPC appendix list for standard one-ply stack-ups. The idea is to make a very simple bill of materials, specifications and notes, and possibly use the same prepreg/resin in the laminate and in the core.

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# It's a Material World

## Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

Years ago, when clock frequencies were low and signal rise times were slow, selecting a dielectric material for your PCB was not difficult; we all just used FR-4. And we didn't really care about the properties of the materials.

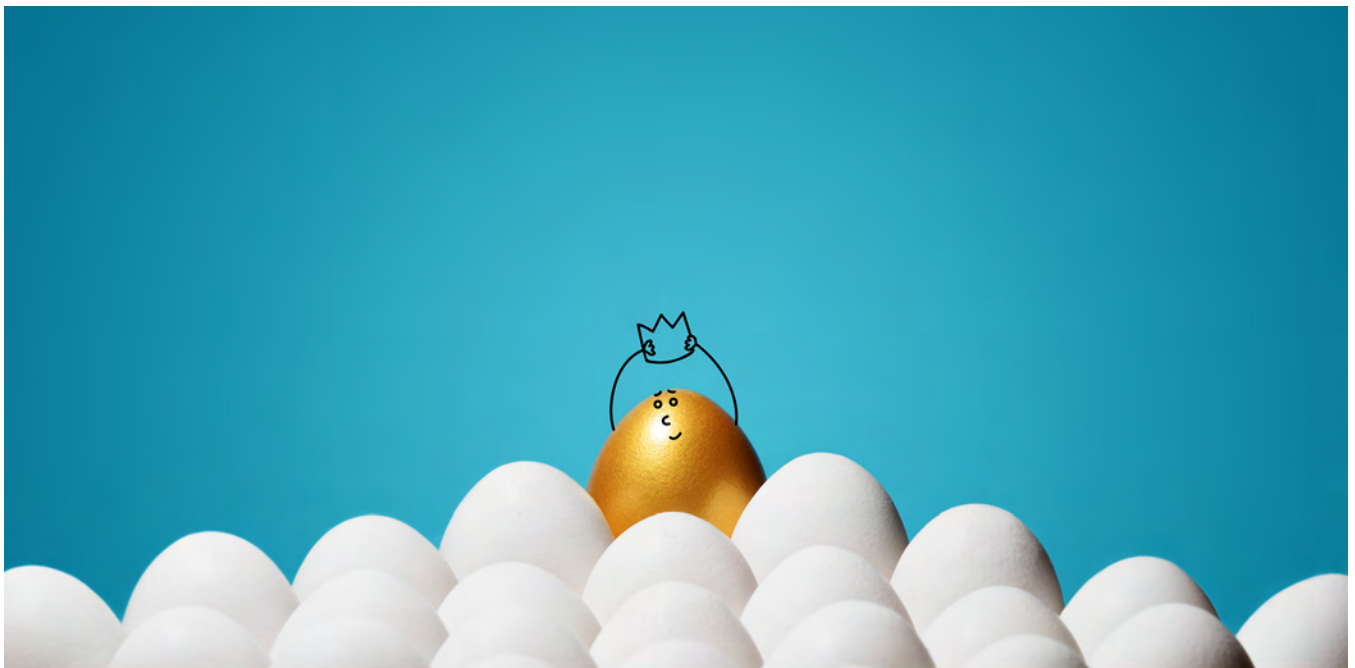
However, with today's multi-gigabit designs and their extremely fast rise times and tight margins, precise material selection is crucial to the performance of the product. Materials used for the fabrication of the multilayer PCB absorb high frequencies and reduce edge rates, and that loss in the transmission lines is a major cause of signal integrity issues. But we are not all designing cutting-edge boards and sometimes we tend to over-specify requirements that can lead to inflated production costs.

Over the years, a huge range of materials have been developed for multilayer PCB fabrication. In fact, to give you an idea, iCD now has a choice of over 700 series of dielectric materials from more than 60 different manufacturers, in its dielectric materials library. When each

material is used for the right target application, the resultant PCB will have the lowest possible cost while still satisfying the design and performance goals of the project. There's no doubt that we live in a material world and selecting the best material for an application is often a daunting task. In this month's column, I will look at how to quickly sort through the vast array of choices to make an informed decision.

The electrical properties of a dielectric material can be described by two terms:

1. The dielectric constant ( $D_k$ ) or relative permittivity ( $\epsilon_r$ ) is the ratio of the amount of electrical energy stored in a material by an applied voltage. It describes how the material increases the capacitance and decreases the speed in the material.
2. The dielectric loss-dissipation factor ( $D_f$ ) or loss tangent ( $\tan \delta$ ) is a parameter of a dielectric material that quantifies its inherent dissipation of electromagnetic energy.





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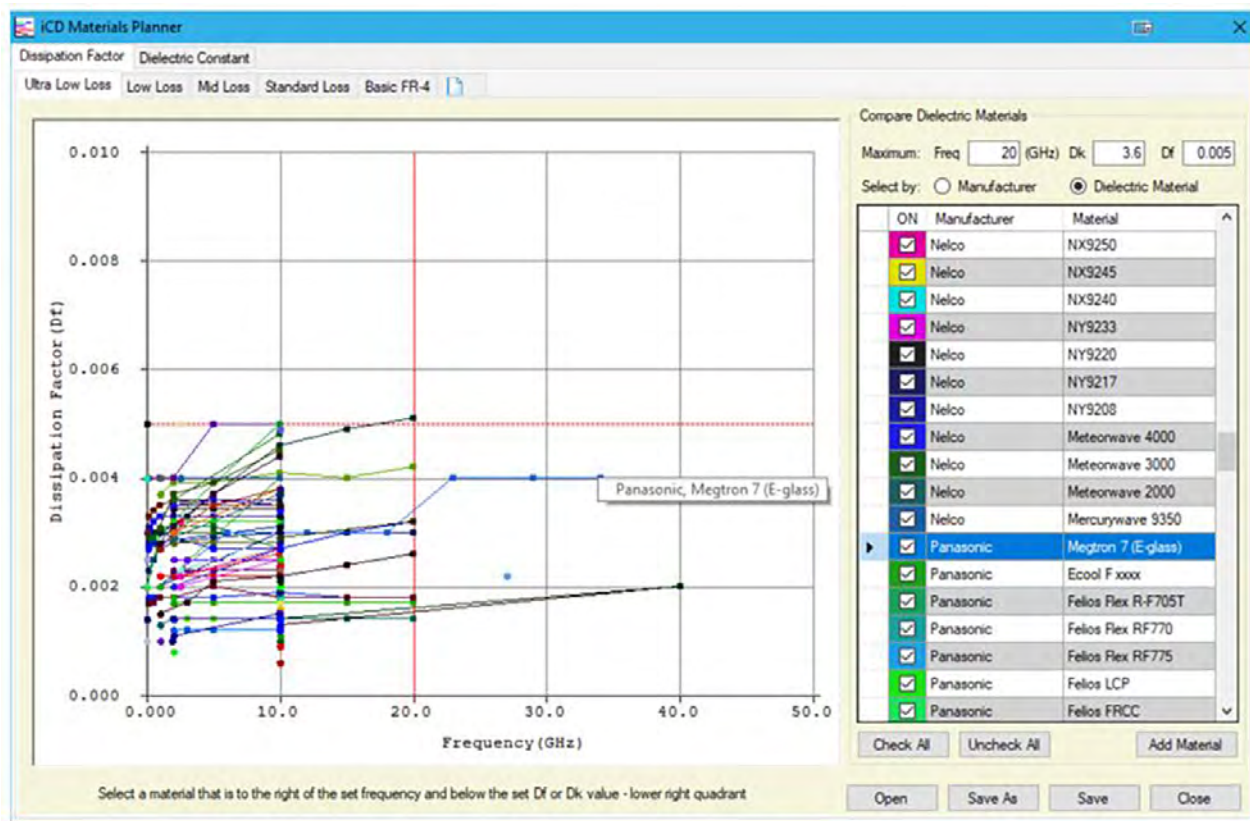


Figure 1: Loss profile for ultralow-loss dielectric materials (source: iCD Materials Planner).

Dielectric constant and dielectric loss are not a function of the geometry of the transmission line—they are a function of the dielectric material in which the signal propagates, their distribution in the PCB stackup, and the applied frequency. These mechanisms contribute to the frequency-dependent loss and degrade the bandwidth and speed of the signal. The signal quality transmitted through the medium and picked up at the receiver will be affected by any impedance discontinuities and by the losses of the dielectric materials.

The glass epoxy material (FR-4) commonly used for PCBs has negligible loss for digital applications below 1 GHz. But at higher frequencies the loss is of greater concern. Also, the entire bandwidth of the signal needs to be considered. For instance, a 10Gbps square wave is made up of a series of odd harmonics. It will have a fundamental frequency of 5GHz, a third harmonic of 15GHz, a fifth of 25GHz and possible higher odd harmonics. These high harmonics can suffer excessive losses in amplitude and a degradation of edge sharpness

which results in distortion of the signal eye. Plus, when the frequency exceeds 1GHz, copper roughness, conductor loss, skin effect and skew, due to variations of glass weave in the dielectric, begin to come into play.

Also of interest is the glass transition ( $T_g$ ) temperature, which is the point at which a glassy solid changes to an amorphous resin/epoxy. If the reflow temperature exceeds the  $T_g$ , for an extended period, the material rapidly expands in the Z-axis. Plus, the mechanical material properties—strength and bonds in the material—degrade rapidly. A high  $T_g$  guards against barrel cracking and pad fracture during reflow. Standard FR-4 has a  $T_g$  of 135-170°C, whereas the high-speed materials are generally over 200°C. Therefore,  $T_g$  is not a factor that needs to be considered for high-speed design but is certainly worth checking.

With so many materials to choose from which is the best for your specific product? Low cost generally means low quality. But also, the price of poor yields drives up the final material cost. Dielectric material selection is usually driven

Profile	Bit Rate (Gbps)	Frequency (GHz)	Dissipation Factor (Df)
Ultralow Loss	$\geq 50$	$\geq 25$	$\leq 0.005$
Low Loss	25 - 50	12.5 - 25	0.005 - 0.010
Mid Loss	10 - 25	5 - 12.5	0.010 - 0.015
Standard Loss	2 - 10	1 - 5	0.015 - 0.02
Basic FR-4	$\leq 2$	$\leq 1$	$\geq 0.02$

Table 1: Loss profile ranges for various materials.

by the frequency and rise time of the digital signal with lower values of loss most suitable for high-frequency applications. These materials generally exhibit lower values of dielectric constant resulting in faster signal propagation.

Figure 1 depicts the profile for dielectric materials with a  $Df < 0.005$ . The iCD Materials Planner has five default profiles ranging from basic FR-4 to ultralow-loss materials as in Table 1. This enables the designer to compare dielectric materials based on manufacturer, fabricator, frequency, dissipation factor (loss) and dielectric constant.

The other issue is that different materials are available locally compared to off-shore and also vary from fabricator to fabricator. Typically,

prototype boards are fabricated locally, whereas Asia is a more economical option for mass production. A profile for each PCB fabricator that you usually deal with can be set up. This will display the complete range of materials that each Fab shop stocks. This also enables the comparison of competitive fab shop capabilities.

Figure 2 plots the loss properties of dielectric materials from an Asian fabricator. One can easily see which materials are best for high-speed applications and can choose a few materials from this that are in stock. Cost-to-performance evaluations must still be done to ensure the lowest cost material, that will do the job, is selected. Also, keep in mind that material costs vary with quantity.

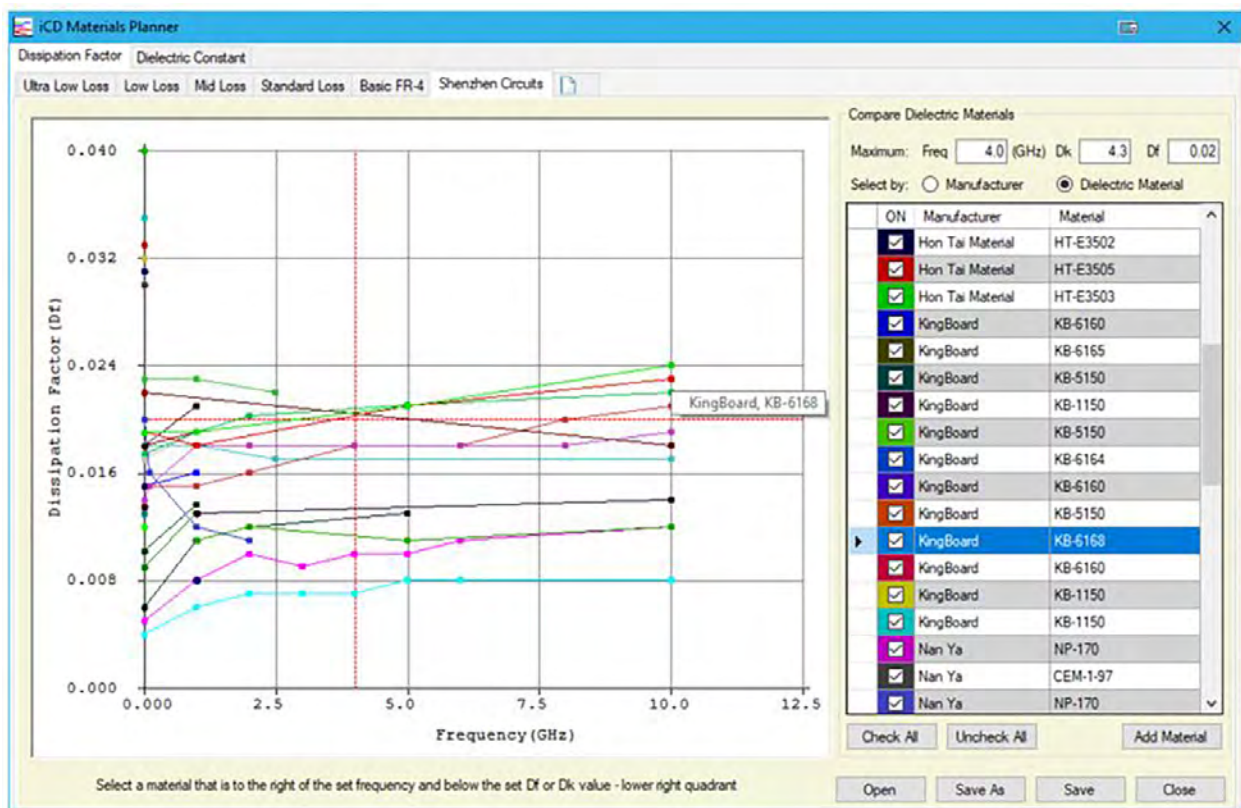


Figure 2: Example of a fabricator's dielectric materials loss profile.

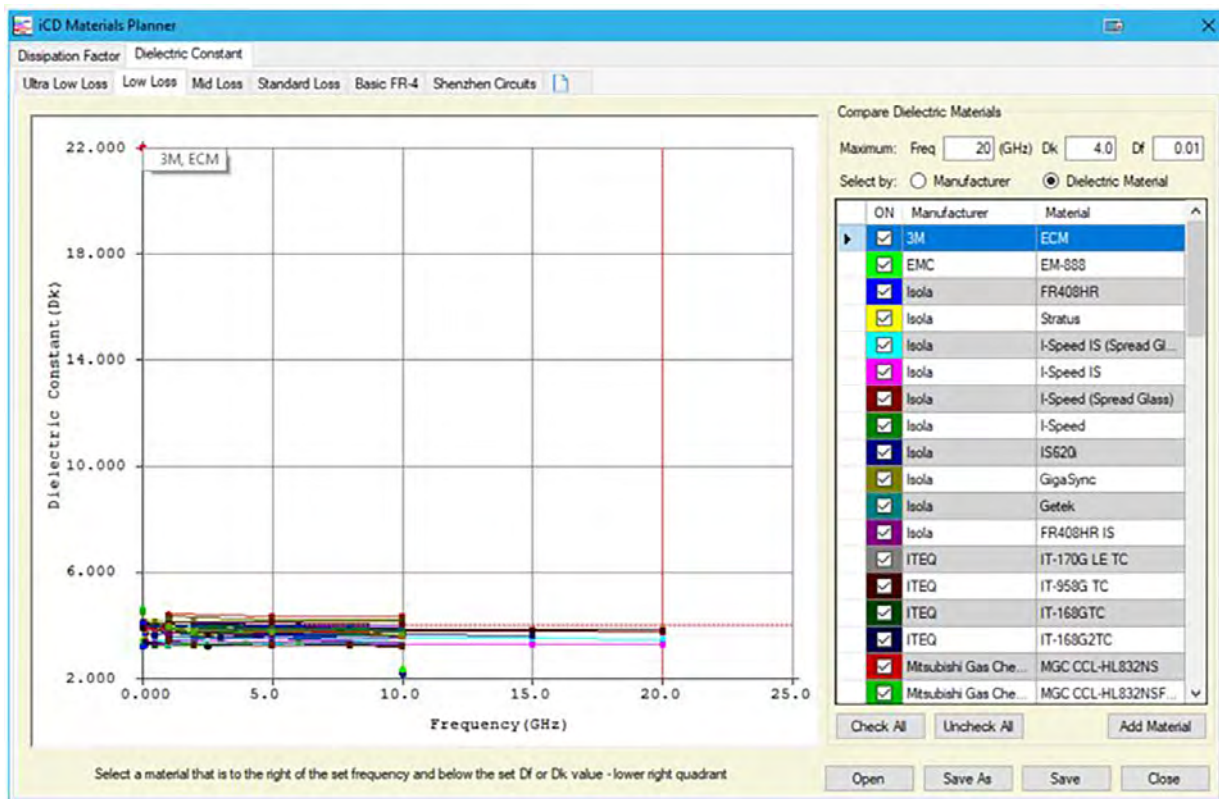


Figure 3: Dielectric constant vs. frequency of low-loss materials.

Matching material performance numbers of the dielectric constant is also important. A small difference in this value between materials can impact impedance, line widths/clearances, and thus losses significantly. Also the dielectric constant, of a material, determines the propagation speed of the signal in the medium. So, if Dk values vary, on different layers of the substrate, then bus timing may also be an issue. One should consider construction options that allow a drop-in material that matches the impedance for each layer of the stackup.

With the continuous trend to smaller feature sizes and faster signal speeds, planar capacitor laminate or embedded capacitor materials (ECMs) are becoming a cost-effective solution for improved power integrity. This technology provides an effective approach for decoupling high-performance ICs whilst also reducing electromagnetic interference.

Embedded Capacitance technology allows for a very thin dielectric layer (0.24 - 2.0 mil) that provides distributive decoupling capacitance and takes the place of conventional discrete decoupling capacitors over 1GHz. Unfortunately,

standard decoupling capacitors have little impact over 1GHz and the only way to reduce the AC impedance of the power distribution network (PDN), above this frequency, is to use ECM or alternatively on-die capacitance. These ultra-thin laminates replace the conventional power and ground planes and have excellent stability of dielectric constant and loss up to 15GHz. As the supply chain grows and becomes more competitive, the costs associated with the use of these materials will continue to decrease which will make system cost reductions possible in a greater number and variety of applications.

Figure 3 outlines the relative dielectric constant of low loss materials. 3M, embedded capacitor material (top left) is the standout. It is a copper clad laminate that utilizes an ultra-thin, high Dk-value dielectric material, between the copper planes, to deliver a capacitance density of up to 20nF/in<sup>2</sup>. Whereas, typical values of Dk, for low-loss materials, vary between 3.2 and 4.0. But, keep in mind that these low loss dielectrics are placed adjacent to signal traces in which case a low Dk is required

to improve signal propagation speed through the medium. However, for planar capacitance, a high Dk creates a high value of capacitance, between the planes, to effectively decouple the PDN at high frequencies.

ECMs offer many benefits when used for decoupling high-speed digital circuits, including:

- Lowers the impedance of the PDN
- Dampens plane resonance
- Reduces power plane noise and thus coupling of plane noise to signals
- Reduces radiated emissions
- Replaces large numbers of discrete decoupling capacitors

From an engineering perspective, noise margins are increased, which can translate into improved performance and less time devoted to troubleshooting and fixing issues further down the track. In addition, the component count reduction saves time in board layout and assembly which reduces cost.

In conclusion, the designer needs to be able to quickly evaluate the best, most cost-effective material for their application based on the vast array of choices available. Sorting through numerous datasheets is a very time-consuming process. And an extensive table of numbers does not paint a memorable picture. However, a direct visual comparison, of dielectric materials, based not only on manufacturer's product lines but more importantly on what one's preferred fabricators stock is undoubtedly the most efficient approach.

## Key Points:

- Materials, used for the fabrication of the multilayer PCB, absorb high frequencies and reduce edge rates causing signal integrity issues.
- Dielectric constant and dielectric loss are a function of the dielectric material, their distribution in the PCB stackup and the applied frequency.
- The glass epoxy material (FR-4) has negligible loss for digital applications below 1 GHz. But, at higher frequencies the loss is of greater concern.

- High harmonics of the fundament can suffer excessive losses in amplitude and a degradation of edge sharpness which results in distortion of the signal eye.
- When the frequency exceeds 1GHz, copper roughness, conductor loss, skin effect and skew, due to variations of glass weave in the dielectric, begin to come into play.
- Standard FR-4 has a Tg of 135°-170°C, whereas the high-speed materials are generally over 200°C.
- Dielectric material selection is usually driven by the frequency and rise time of the digital signal with lower values of loss most suitable for high frequency applications.
- A small difference in dielectric constant between materials can impact impedance, line widths and clearances, and thus losses significantly.
- Embedded capacitance technology provides distributive decoupling capacitance and takes the place of conventional discrete decoupling capacitors over 1GHz.

## References

1. Barry Olney's Beyond Design columns: [Material Selection for Digital Design](#), [Material Selection for SERDES Design](#), [Effects of Surface Roughness on High-Speed PCBs](#).
2. [Selecting PCB Materials for High-Speed Digital Circuits](#), by John Coonrod, Rogers Corporation.
3. [Using Embedded Capacitance to Improve Electrical Performance](#), by Joel Peiffer, 3M.



**Barry Olney** is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN and CPW Planner. The software can be downloaded from [www.icd.com.au](http://www.icd.com.au). To contact Olney, or read past columns, [click here](#).

# Transitioning from FR-4 to High-Frequency Materials, Revisited

**Lightning Speed Laminates**  
by John Coonrod, ROGERS CORPORATION

This is a topic I have written about a few times, most recently in my [August 2017 column](#), and with good reason. The answer, “it depends,” typically annoys engineers; fortunately, there is a list of items that can help the PCB designer answer the question of when to transition from FR-4 to high-frequency materials.

The bottom line is that FR-4 materials have been around a long time, and they work well within their formulated range. The same can be said for high-frequency circuit materials, which are also thought of as low-loss materials. However, there is a definite gray area that can muddy the waters when a designer is weighing a possible decision to switch from

FR-4 to low-loss materials. High-frequency materials also have inherent properties that can benefit some applications that are not related to high frequencies or low loss. The material property differences between FR-4 and high-frequency materials is critical for the designer to understand when considering the use of either material.

It may be a good idea to compare properties of FR-4 to a commonly used high-frequency material. The low-loss material to be considered here is the RO4835 laminate. The FR-4 material that will be examined is a higher-quality, high-Tg FR-4 material. This comparison is mostly meant to trigger a designer’s thought process; there are admittedly exceptions with





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Property	FR-4	High-frequency Material
Dk control	poor	good
Df control	poor	good
Circuit fabrication	excellent	moderate
Thickness control	moderate	good
Moisture absorption	moderate	excellent
Thermal conductivity	poor	excellent
TCDk	poor	excellent

Table 1: A subjective rating of material properties.

these materials and the properties mentioned. Following is my subjective rating as a list of material properties for this comparison in Table 1.

The first item, Dk control (control of dielectric constant property), is very well controlled for high-frequency materials and not so well controlled for FR-4. For applications at lower frequencies, the lack of Dk control is often not a concern, but there are exceptions. Even lower-frequency circuits sometimes need well controlled impedance and having Dk that is tightly controlled can be advantageous for getting better yields with a controlled-impedance board.

Having good control of the Df property for low-frequency applications is typically not a concern. However, when the designer is considering FR-4 for an application where insertion loss is a concern, the inconsistency of FR-4 may preclude the designer from understanding the true limits of that material.

Circuit fabrication can impact the cost of the circuit as well as the consistency of different circuit properties. FR-4 materials are defined very well in the PCB fabrication process and are typically not a concern. The high-frequency material chosen for this example is defined well in the PCB fabrication process, but there are different parameters which must be used for fabricating with this material, and these parameters can make the circuit fabrication costlier.

Because the same FR-4 substrates are often manufactured differently at different manufacturing sites, this can certainly impact the thickness control of the substrate. The lot-to-lot (or

within lot) variation of thickness control is typically much worse for FR-4 than for high-frequency materials. But thickness control of the substrate is extremely important to high-frequency designs. High-frequency materials are tightly controlled in the manufacturing process to provide consistent substrate thickness tolerance, because this tolerance has a direct impact on critical high-frequency circuit functions such as impedance, phase response, bandwidth

and insertion loss. High-frequency materials with their tightly controlled thickness tolerance help improve yields for controlled-impedance boards, which leads to cost savings.

Moisture absorption is another important aspect to ensure consistent high-frequency performance, which is well defined in the formulation of most high-frequency circuit materials. Moisture absorption for a low-frequency application may or may not be important. In some cases, having a low moisture-absorbing material in a dynamic operating environment may not be an electrical concern. However, it could be a reliability concern. There are low-frequency applications that have no issues with electrical performance, but still utilize a high-frequency circuit material to avoid issues with moisture absorption.

Several applications have a board-mounted chip or device, which generates heat during normal operation. Using high-frequency materials with higher thermal conductivity can minimize thermal management concerns. The typical FR-4 material has a thermal conductivity property of about 0.25 W/m/K as compared to RO4835, which has a thermal conductivity of 0.62 W/m/K. This is a difference of more than 2X, which can certainly have a positive impact on thermal management.

Even with low-frequency circuits, when electrical consistency is required, the thermal coefficient of Dk (TCDk) must be considered. In a nutshell, TCDk is a measurement of how much the Dk of the substrate will change, given a change in temperature. FR-4 materials are not formulated with this property in mind and because of that, it is not uncommon for these

materials to have TCDk values of more than 300 ppm/°C. The general rule of thumb in the high-frequency industry is that the TCDk should not be greater than 50 ppm/°C, which is the TCDk value for the RO4835 laminate.

Aside from the previously mentioned concerns, the tradeoffs between FR-4 and high-frequency materials often comes down to insertion loss differences. Some tricks can be done to get FR-4 to provide better loss performance at higher frequencies. One is to have the FR-4 laminate use a very smooth copper. The surface of the copper that is of concern is the copper surface roughness at the copper-substrate interface. Smooth copper at this interface will reduce the conductor loss, which is a component of the overall insertion loss. Also, if the FR-4 substrate is relatively thin, the conductor effects will be more significant, and the smooth copper will help improve insertion loss. The poor dissipation factor (Df) for FR-4 is really a big issue for insertion loss. In general, a high-Tg FR-4 substrate usually has Df values of 0.015 to 0.025 when tested at 1 GHz, as compared to the high-frequency material in these comparisons, which has a Df value of about 0.0025 at 1 GHz.

Whether or not FR-4 is acceptable for insertion loss will need to be addressed by the PCB designer who is familiar with the limits of the loss budget. Remember that when dealing with the gray area between FR-4 and high-frequency laminates, another choice is available: mid-loss materials. These materials typically have a Df value of 0.005 to 0.015 at 1 GHz and their laminate costs are usually closer to the cost of high-frequency materials costs than FR-4. The Rogers Kappa 438 laminate is considered a mid-loss material. It has a lot of the properties of high-frequency laminates, but it also has a Dk value that is closely matched to FR-4, with a much lower Df than FR-4 that is not as good as that of the RO4835 laminate.

When it's time to move from FR-4 to a high-frequency material, keep in mind that you always have options. **DESIGN007**



**John Coonrod** is technical marketing manager of Rogers Corporation. To read his past columns or to contact Coonrod, [click here](#).

## Smart Homes Open New Approaches and Business Models for Healthcare Delivery

As healthcare shifts to proactive care, a huge market is opening for automation products that can help deliver health and wellness services through smart homes. The ubiquity of broadband connectivity, development of smart sensors, and the decreasing costs of devices have already made it possible to offer aging-in-place, chronic disease management, and post-acute care services in smart homes. However, digital health vendors are striving to take telehealth to the next level by developing solutions that will allow care givers to check on the health of all the residents of the house, not just the patient's, monitor diet and nutrition, environment, and be integrable with existing and newer systems.

"Patients are conscious of their health and want to be involved in the wellness and disease management," said Sowmya Rajagopalan, global program director, Transformational Health. "With consumerization of healthcare, enabling patients to clinically manage their disease at home has been of crucial importance for care providers and OEMs today as they have made this a reality with the launch of innovation in design, devices, services, and solutions."

Frost & Sullivan's recent analysis, Vision 2025—Healthcare in the Smart Home, examines the concept of a smart home delivering healthcare. It segments resident profiles and lists the individual needs that are relevant to healthcare delivery in the home.

Source: Frost & Sullivan



# Testing Time for Resins

Sensible Design

by Alistair Little, ELECTROLUBE

Earlier this year, I began my new series of columns on resins. I selected five frequently asked questions that I hear from customers on such subjects as resin chemistries and properties and typical resin applications and their limitations. I followed this up in a later column by compiling what I believe are the five top tips for those circuit designers and manufacturers who are frequent specifiers and users of resins and want to get the best out of them.

This month, my column has a bit of a testing theme running through it, and I include my responses to more technically probing questions. In no particular order, here are five questions from customers that raise several technical issues related to resin applications, together with my responses. Hopefully, it will provide useful background information to help you with your own problem-solving activities.

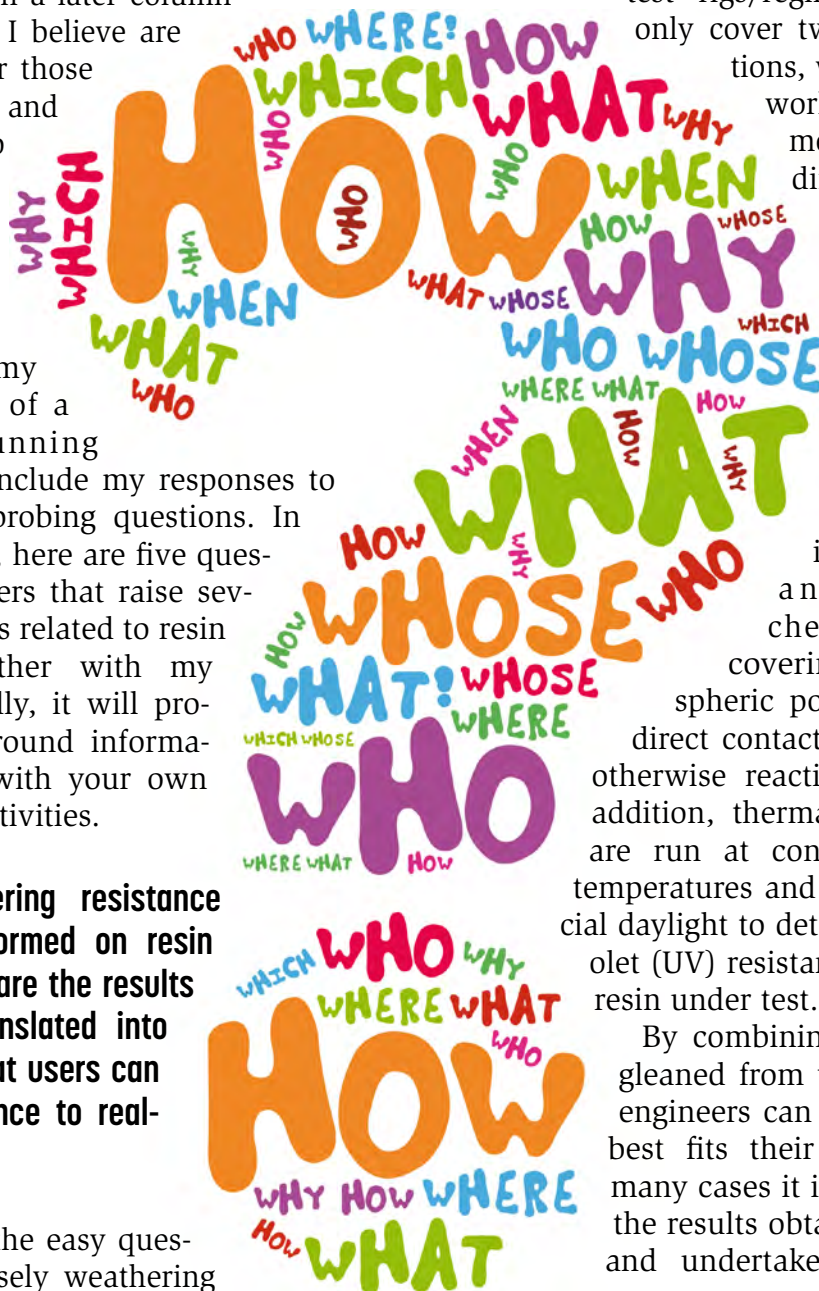
**Q. What weathering resistance tests can be performed on resin products, and how are the results of these tests translated into meaningful data that users can apply with confidence to real-world applications?**

**A.** Let's address the easy question first. How closely weathering

test data relates to the real world has been exercising the minds of both the suppliers and users of resins since weathering tests were first developed. The main problem here is that a weathering (environmental and mechanical exposure) test rigs/regime will, at best, only cover two or three conditions, whereas in the real world, things are far more complex and difficult to predict.

Testing is a fundamental process. Electrolube carries out a range of thermal cycling (checking thermal shock resistance), water immersion (fresh and salt), and chemical resistance, covering both atmospheric pollution as well as direct contact with corrosive or otherwise reactive substances. In addition, thermal stability checks are run at continuous operating temperatures and exposure to artificial daylight to determine the ultraviolet (UV) resistance/stability of the resin under test.

By combining the information gleaned from these tests, design engineers can select a resin that best fits their requirements. In many cases it is possible to input the results obtained into a model and undertake a FEMA study,



# Rogers' Laminates: Paving the way for tomorrow's Autonomous Vehicles

Autonomous “self-driving” vehicles are heading our way guided by a variety of sensors, such as short and long range radar, LIDAR, ultrasound and camera. Vehicles will be connected by vehicle-to-everything (V2X) technology. The electronic systems in autonomous vehicles will have high-performance RF antennas. Both radar and RF communication antennas will depend on performance possible with circuit materials from Rogers Corporation.

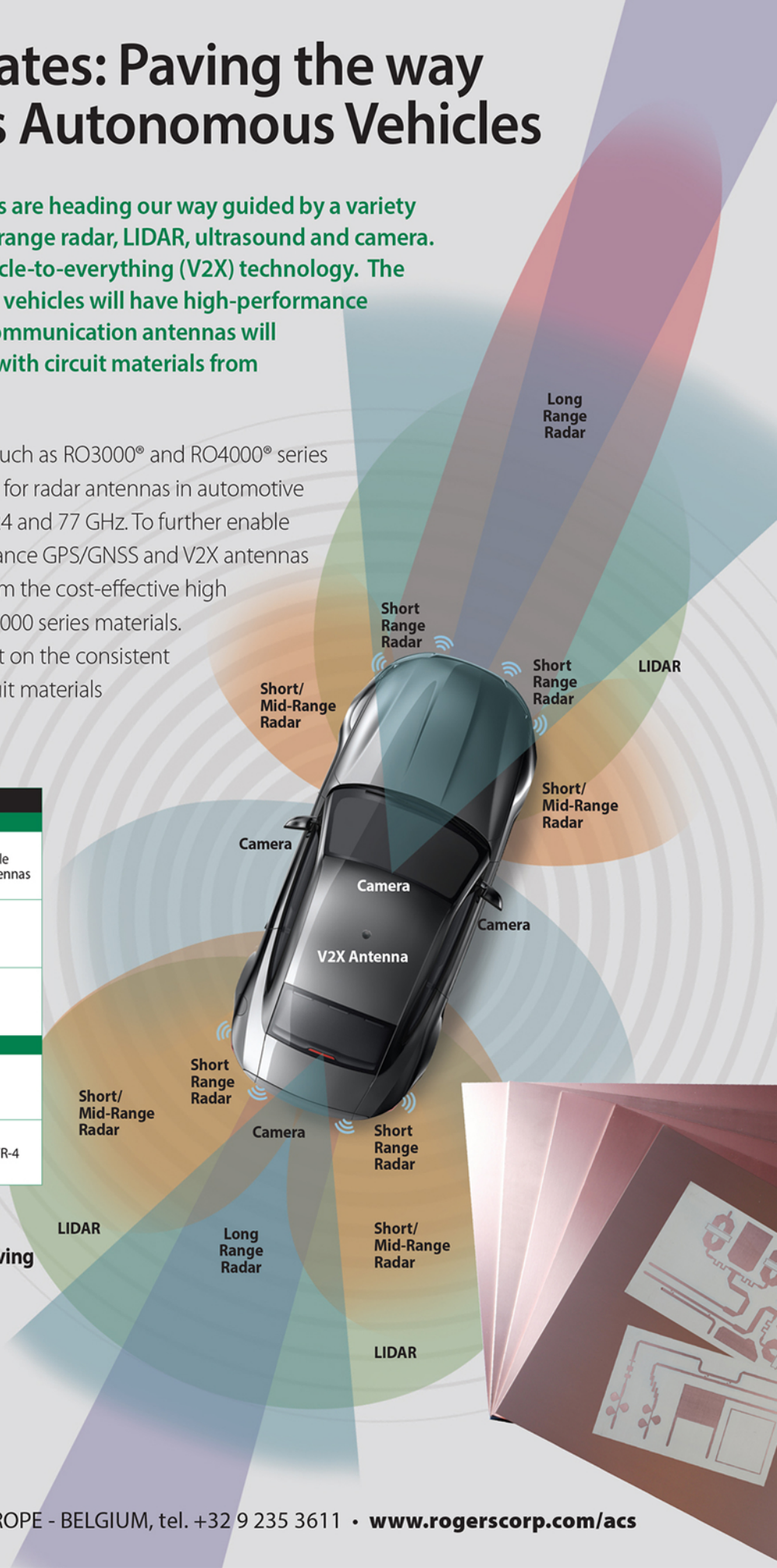
High-performance circuit laminates, such as RO3000® and RO4000® series materials, are already well established for radar antennas in automotive collision-avoidance radar systems at 24 and 77 GHz. To further enable autonomous driving, higher performance GPS/GNSS and V2X antennas will be needed, which can benefit from the cost-effective high performance of Kappa™ 438 and RO4000 series materials. These antennas and circuits will count on the consistent quality and high performance of circuit materials from Rogers.

Material	Features
RADAR	
RO3003™ Laminates	Lowest insertion loss and most stable electrical properties for 77 GHz antennas
RO4830™ Laminates	Cost-effective performance for 77 GHz antennas
RO4835™ Laminates	Stable RF performance for multi-layer 24 GHz antennas
ANTENNA	
RO4000 Series Circuit Materials	Low loss, FR-4 processable and UL 94 V-0 rated materials
Kappa™ 438 Laminates	Higher performance alternative to FR-4

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where the environmental conditions are one consideration in predicting the long-term performance of the final product. The results from the test conditions ensure that the user can expect optimal performance from our products in a range of environments.

**Q. Which industries typically ask for resins that are designed to perform well in RF applications, and what is so special about these resins?**

**A.** Typically, the communications industry (manufacturers of mobile and fixed telecommunications equipment) is most likely to specify a resin that is specially formulated to protect electronic assemblies that generate RF signals. However, many other companies are now adding Wi-Fi/Bluetooth functionality to a much wider range of products to facilitate easy communication between devices.

Resins designed for RF applications do not contain fillers—particles that might otherwise cause RF signal scattering or attenuate the signal altogether. In many cases the transmission power of devices utilising Wi-Fi/Bluetooth is quite low, so any intervening medium, such as a protective resin, which might reduce or scatter the signal strength, is a potential problem.

Flame retardancy is often specified for RF applications but most flame-retardant resins will either contain halogens (which are now facing increasing regulatory restriction) or metal containing fillers (that scatter or attenuate RF signals). We have met this challenge with the UR5641/2/3 series of flame-retardant, filler-free and halogen-free resins that are suitable for a wide range of RF applications.

**Q. When is it important to ensure that a resin's dielectric constant does not vary over the long term?**

**A.** Dielectric constant (also known as relative permittivity) is an important parameter when resins are concerned. A resin with low dielectric constant, for example, will have minimal impact on any electric field produced by a device and thus ensure maximum transparency for any signals generated by that device. It

is also important that the resin's dielectric constant remains low over the entire life of a product or system to which it has been applied. In the case of marine applications, for example, a resin's consistent long-term electrical performance may be critical, as having to replace units compromised by dielectric constant variability is likely to be operationally costly, particularly if those units are in difficult-to-access areas, such as the bottom of the ocean.

**Q. How does Electrolube measure thermal conductivity and why is the accuracy of the testing method so important?**

**A.** We have recently invested in some new thermal conductivity measurement equipment that uses the Modified Transient Plane Source method of measuring thermal conductivity, (an improvement upon the well-known Hot Disk Transient Plane Source method), which has been well established over the years. This enables us to obtain many measurements over a wide temperature range quickly and reliably.

Direct measurements of a thermal paste or cured resin provide values for thermal conductivity that are very close to those experienced under real operating conditions; however, there will always be some slight variation due to the nature of the design of the unit and the components used. Unfortunately, there are still cases where the thermal conductivity of a cured resin will have been calculated from the component parts, rather than having been obtained from a measurement of the material. Calculated values are generally far higher than those obtained from direct measurement of the materials in question.

**Q. When is it appropriate to consider using a single- vs. a two-component resin system?**

**A.** Single-component resins (or 1K resins) are generally used for adhesive applications such as a glob top, or for bonding components to a PCB or other substrates. A 1K resin does have its disadvantages, however. Viscosity is generally higher than that of its 2K counter-

part, it requires an elevated cure temperature, will have a short shelf life, and often needs to be stored in a chilled environment. The main advantage of a 1K resin is its ease of application; no mixing is required, and dispensing machine set up is a much simpler affair.

Over the coming months, I shall be sharing this column with my colleagues who will be covering other areas of electronic circuit protection. In the meantime, I hope to cover a wide range of issues concerning the correct

choice and application of resins and provide answers to many of your resin related questions, so be sure to keep an eye out for future columns. **DESIGN007**



**Alistair Little** technical director of Electrolube's Resins Division.

## EMA Expands Library with Power Integrations EDA and MCAD Models

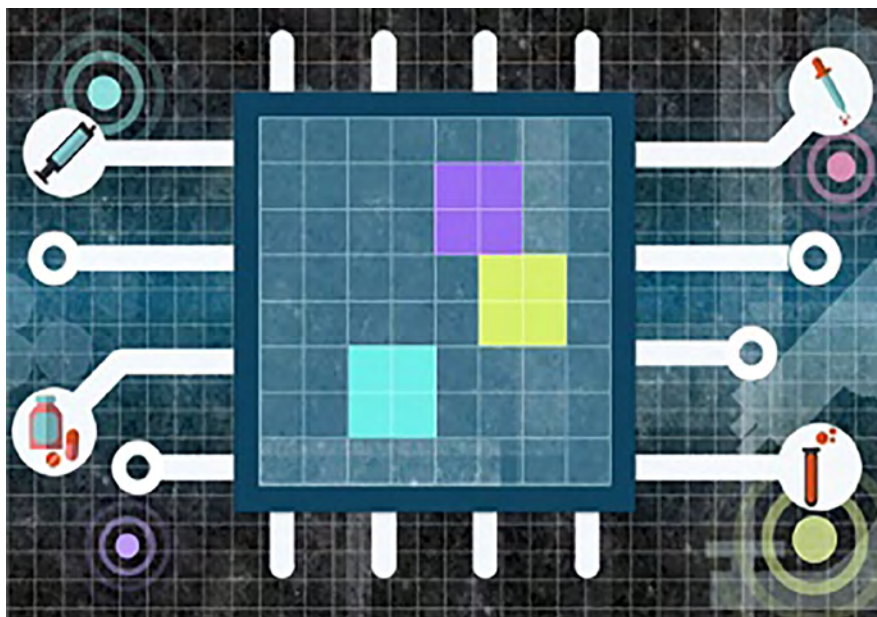
EMA Design Automation announced the availability of symbols, footprints, and 3D models for all Power Integrations components and anyone can access for free from [ultralibrarian.com](http://ultralibrarian.com), [power.com](http://power.com), and [digikey.com](http://digikey.com). "With this new set of models, engineers can download the library components they need for their Power Integrations based designs," said Manny Marcano, president and CEO of EMA. "Having access to these verified models saves engineering time and eliminates mistakes that can occur when manually building part models."

Power Integrations' high-performance electronic components are important to engineers designing high-voltage power-conversion systems. These integrated circuits and diodes enable compact, energy-efficient AC-DC power supplies for a wide range of electronic products including mobile devices, televisions, computers, appliances and smart utility meters.

"We chose to provide Ultra Librarian based models for Power Integrations components because we wanted the highest quality design models possible, and we wanted it freely available to the widest audience," said David Chen, director of applications engineering for Power Integrations. "Giving our customers the ability to download design-ready, verified models allows them to easily and correctly create designs using our high-performance electronic components."

All models are created based on Power Integrations specifications, and the symbols, footprints, and 3D models are built to function correctly together. All features such as matching pin names and numbers, accurate cross-probing between symbols and footprints, and 3D models are precisely aligned with the footprints. The models go through more than 30 checks during creation by the Ultra Librarian team and are then verified by Power Integrations engineers. The Ultra Librarian 3D models are more accurate than generic 3D models—important when there are tight space requirements. The Power Integrations models are downloadable in over 20 CAD formats and available for almost all EDA and CAD design tools.

Source: EMA Design Automation





# MilAero007 Highlights



## It's Time to Retire ROSE Testing ►

The transition from predominantly water wash processes to “no clean” has meant the advent of very different flux compositions. The question has been posed as to whether the ROSE test is still a viable option for evaluating PCB and PCBA cleanliness.

## Global Electronic Warfare Market to See CAGR of 6.2% from 2017-2026 ►

The Global Electronic Warfare market is accounted for \$22.19 billion in 2017 and is expected to reach \$38.31 billion by 2026, growing at a CAGR of 6.2%.

## Compass Call Electronic Warfare System Moving to Modern Business Jet ►

BAE Systems has begun work to transition its advanced Compass Call electronic warfare (EW) system from aging EC-130H aircraft to a modern, more capable platform that will improve mission effectiveness.

## Solving the Challenges of 'Flying Microgrids' ►

As the role of satellites for communications, navigation, research and defense continues to grow, researchers say there is a need to address a number of unique challenges faced by satellite power systems.

## Digital Transformation Key to Survival in Aerospace & Defense ►

Despite solid profits in recent years and a decade of stock market outperformance, the global aerospace and defense (A&D) industry cannot afford to be complacent in the face of an increasingly dynamic business environment.

## Electronics Industry Supports Senate Bill to Advance Workforce Education ►

IPC—Association Connecting Electronics Industries, representing the \$2 trillion global electronics industry, applauds a U.S. Senate committee for its work in advancing a workforce education and training bill.

## Lyncolec Receives prEN9100:2016 (AS9100D) Certification ►

SCL PCB Solutions Group announced that its manufacturing subsidiary Lyncolec has been awarded with certification for prEN 9100:2016 (technically equivalent to AS9100D and JISQ 9100:2016) and ISO9001:2015.

## Nano Dimension Partners With AURORA Group for China Distribution ►

Nano Dimension has entered the Chinese market with a strategic partnership with the AURORA Group. The AURORA Group will market and sell Nano Dimension's award-winning DragonFly 2020 Pro 3D printer for electronics to customers in China.

## Cirexx Achieves AS9100D Certification ►

Cirexx International has acquired AS9100D Standard Certifications in only four months. The AS9100 Quality Management System (QMS) is a rigorous standard for organizations that design and manufacture products for the defense and aerospace industries.

## Collaborative Robots and Digital Technology Signal Creation of the 'Factory of the Future' ►

The cobotic workstation, a key feature of the factory of the future, is fitted with a range of digital technology and will be piloted at the company's Warton, Lancashire site.



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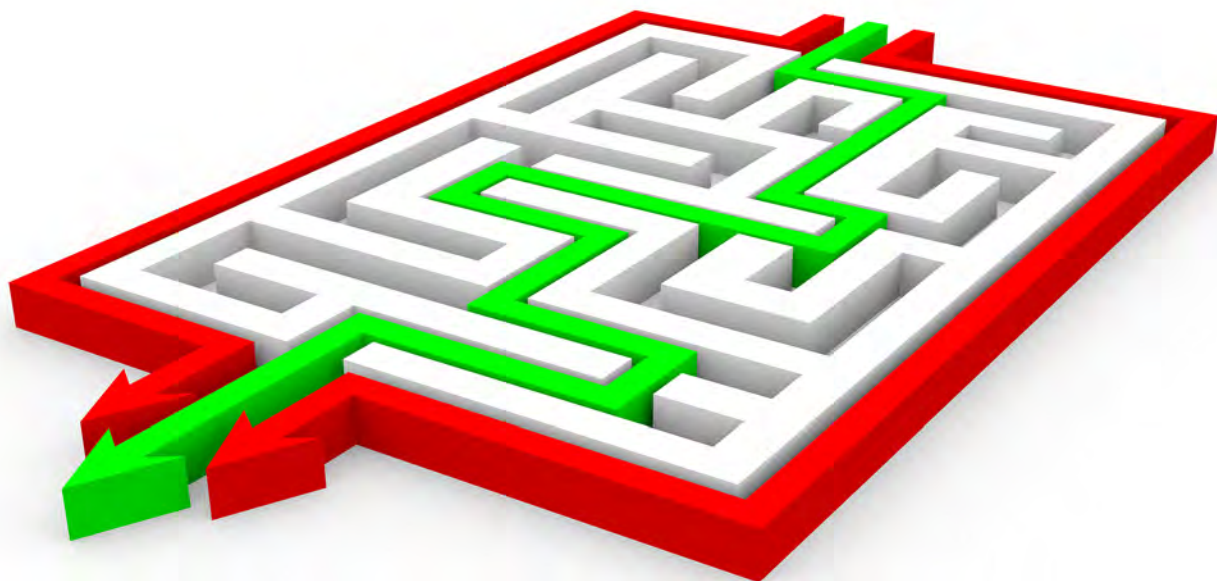
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# The Impact of PCB Dielectric Thickness on **Signal Crosstalk**

**Article by Chang Fei Yee**  
KEYSIGHT TECHNOLOGIES

This article studies the impact of dielectric thickness on crosstalk for transmission lines in single-ended and differential mode on outer (microstrip) and inner (stripline) PCB layers. Crosstalk analysis is performed in 2D simulation and S-parameters are subsequently observed.

## Introduction to Crosstalk

Crosstalk is an unintentional electromagnetic (EM) field coupling between transmission lines on a PCB. This phenomenon becomes a major culprit in signal integrity (SI), contributing to the rise of bit error occurrence in data communications and electromagnetic interference (EMI). With the existence of mutual inductance and capacitance between two adjacent transmission lines on a PCB, crosstalk has become more severe due to the shorter signal rise/fall times at today's higher data speed rates.

With reference to Equation 1, crosstalk can be minimized by routing the PCB traces fur-

ther apart and reducing the dielectric thickness between PCB trace and reference plane <sup>[1, 2]</sup>. We will observe how a PCB's dielectric thickness affects the signal crosstalk. All crosstalk analyses are carried out in 2D simulation using Mentor's HyperLynx.

Equation 1:

$$X_{talk} = \frac{1}{1 + \left(\frac{D}{H}\right)^2}$$

D = Spacing between PCB traces

H = Dielectric thickness between PCB trace and reference plane

## Analysis of Crosstalk in 2D Simulation

In this study, eight 2D transmission line models in single-ended and differential mode on outer (microstrip) and inner (stripline) PCB layers are constructed based on varying PCB dielectric thickness. Figure 1 depicts the crosstalk simulation topology for each transmission line model (i.e., single-ended mode) listed in Table 1. The transmitting and receiving ends of

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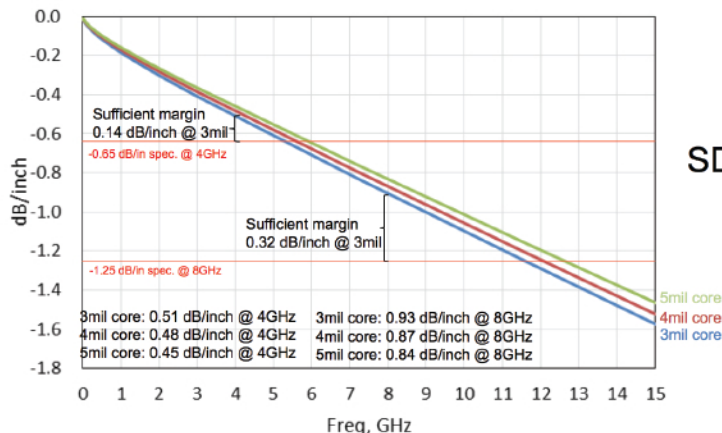
### Feature

### Purley Platform Mid-Loss Solution – Hi Tg

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Items	Methods	IT-170GRA1
Tg (°C)	DSC	180
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Td-5%(°C)	TGA 5% loss	380
CTE (%), 50-260°C	TMA	2.4
Peel strength (lb/inch)	1 oz	7.0
Water absorption	D-24/23	0.1
Dk: 2-10 GHz	Bereskin	3.96 – 3.99
Df: 2-10 GHz	Bereskin	0.0073 - 0.0075

## IT-170GRA1 Insertion Loss



SDD21

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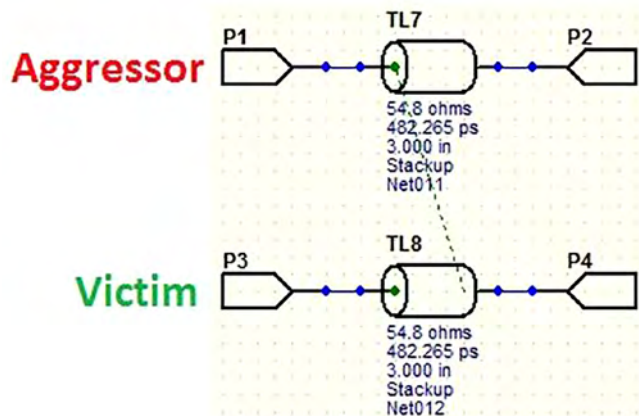


Figure 1: Crosstalk simulation topology for transmission line models listed in Table 1.

the aggressor line are assigned as port P1 and P2, respectively, while the transmitting and receiving ends of the victim line are assigned as port P3 and P4, respectively. The coupled spacing and length between the aggressor and victim are set triple the trace width and 3 inches, respectively.

These four transmission line models are created with medium-loss substrate material (i.e., 3.6 Dk and 0.01 Df). Each model has a trace thickness of .0012". Model 1A is set as microstrip, with a substrate thickness .003" and trace width .007" to achieve a characteristic impedance of 45.1 ohms. Meanwhile, model 1B has the same parameter setting as 1A except the substrate thickness is increased to .004" to achieve a characteristic impedance of 53.7 ohms. The substrate thickness of model 1B is increased by not more than .001" versus model 1A to limit the trace impedance of both models to within  $\pm 10\%$  tolerance of the nomi-

nal 50 ohms. The interest of this study is on varying substrate thickness, hence the other parameters of both model 1A and 1B shall remain the same.

On the other hand, model 2A in Table 1 is set as a symmetrically centered stripline, with a trace width of .005" and a substrate thickness of .005" between the trace and upper/lower reference plane, to achieve characteristic impedance of 45.7 ohms. Meanwhile, model 2B has the same parameter setting as 2A except substrate thickness between trace and upper/lower reference plane is increased to .007", to help achieve characteristic impedance of 54.8 ohms (i.e., within  $\pm 10\%$  tolerance of the nominal 50 ohms).

By field solving the four-port simulation topology depicted in Figure 1, the S41 parameter that represents far-end crosstalk of the transmission line models in Table 1 are plotted in Figure 2 (from 1MHz to 30GHz). Most data communication protocols in embedded systems are source synchronous, where high-speed signals propagate in the same direction at any one time. We are concerned about the ratio of induced noise at the victim's receiving end to the injected signal at the adjacent aggressor's transmitting end (i.e., S41 parameter). A more severe crosstalk is indicated by smaller absolute value in dB.

With reference to Figure 2, across the wideband up to 30GHz, the S41 for model 1A is about 3dB lower than 1B. Similarly, the S41 for model 2A is at least 8dB lower versus 2B. This result indicates that for both microstrip and stripline in single-ended mode, a thinner

T-line model	mode	T-line medium	Dk	Df	dielectric thickness between signal and plane (mil)	trace thickness (mil)	trace width (mil)	Zo (ohm)	Xtalk coupled spacing (mil)	Xtalk coupled length (inch)
1A	single ended	microstrip	3.6	0.01	3	1.2	7	45.1	21	3
1B	single ended	microstrip	3.6	0.01	4	1.2	7	53.7	21	3
2A	single ended	symmetrically centred stripline	3.6	0.01	5	1.2	5	45.7	15	3
2B	single ended	symmetrically centred stripline	3.6	0.01	7	1.2	5	54.8	15	3

Table 1: 2D transmission lines in single-ended mode for varying dielectric thicknesses modeled.

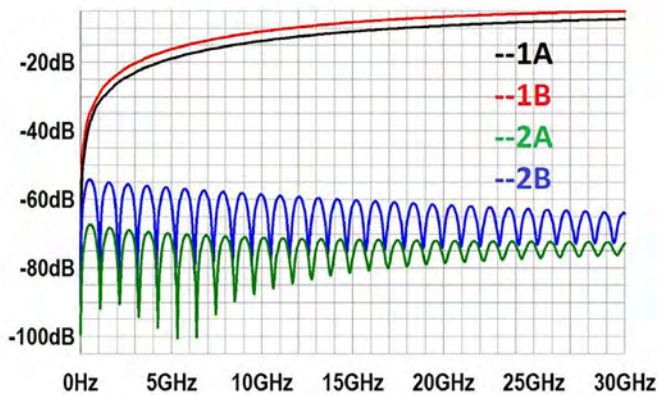


Figure 2: Simulated plots of far-end crosstalk for transmission line models listed in Table 1.

substrate or dielectric between the PCB trace and the adjacent reference plane reduces signal crosstalk.

The crosstalk analysis is continued with simulation topology depicted in Figure 3 for each transmission line model (i.e., differential mode) listed in Table 2; the transmitting end of the aggressor's positive and negative lines are assigned as port P1 and P2, respectively, while receiving end of the victim's positive and negative lines are assigned as port P3 and P4, respectively. The receiving end of the aggressor pair and transmitting end of victim pair are terminated. The coupled spacing and length between the aggressor and victim are set triple the trace width and 3 inches, respectively.

These four transmission line models are laminated with medium-loss substrate material (i.e., 3.6 Dk and 0.01 Df). Each model has a trace thickness of .0012". Model 3A is set as microstrip, with a substrate thickness of .003",

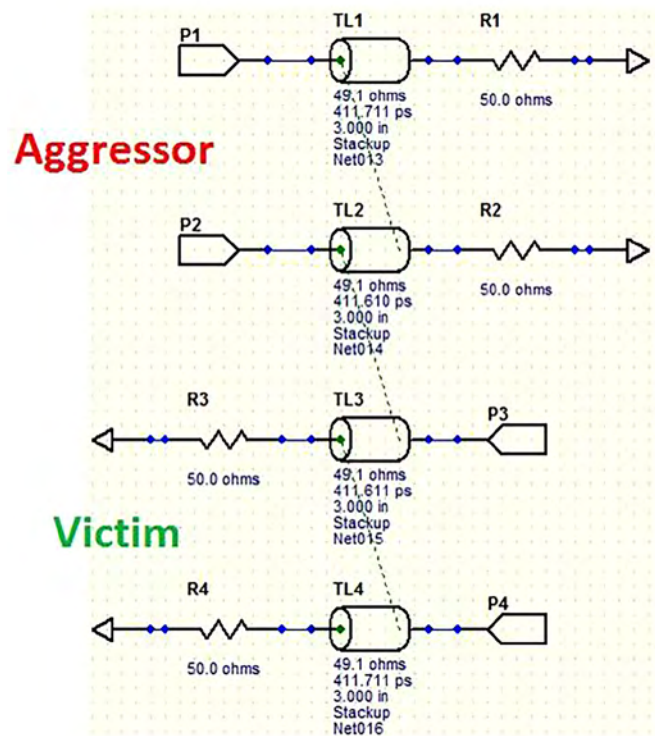


Figure 3: Crosstalk simulation topology for transmission line models listed in Table 2.

trace width of .006", and intra-pair spacing of .008" to achieve characteristic impedance of 92.1 ohms. Meanwhile, model 3B has the same parameter setting as 3A, except the substrate thickness is increased to .004" to achieve characteristic impedance 105.8 ohms. The substrate thickness of model 3B is increased by not more than .001" versus model 3A to limit the trace impedance of both models within  $\pm 10\%$  tolerance of the nominal 100 ohms.

On the other hand, model 4A in Table 2 is set as a symmetrically centered stripline, with

T-line model	mode	T-line medium	Dk	Df	dielectric thickness between signal and plane (mil)	trace thickness (mil)	trace width (mil)	intra-pair spacing (mil)	Zdiff (ohm)	Xtalk coupled spacing (mil)	Xtalk coupled length (inch)
3A	differential	microstrip	3.6	0.01	3	1.2	6	8	92.1	18	3
3B	differential	microstrip	3.6	0.01	4	1.2	6	8	105.8	18	3
4A	differential	symmetrically centred stripline	3.6	0.01	5	1.2	4.5	8	91.2	13.5	3
4B	differential	symmetrically centred stripline	3.6	0.01	7	1.2	4.5	8	103.2	13.5	3

Table 2: 2D transmission lines in differential mode for varying dielectric thickness.

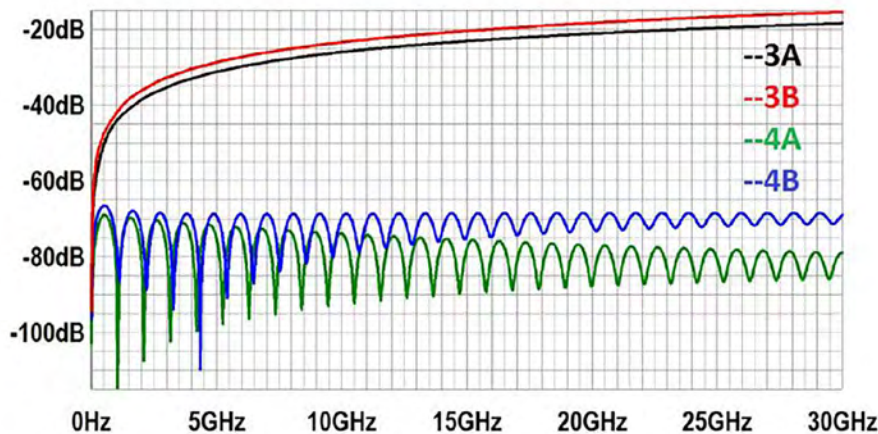


Figure 4: Simulated plots of far-end crosstalk for transmission line models listed in Table 2.

a trace width of .0045", intra-pair spacing of .008", and substrate thickness of .005" between trace and upper/lower reference plane, to achieve characteristic impedance of 91.2 ohms. Meanwhile, model 4B has the same parameter setting as 4A, except the substrate thickness between the trace and upper/lower reference plane is increased to .007", to achieve characteristic impedance of 103.2 ohms (i.e., within  $\pm 10\%$  tolerance of the nominal 100 ohms).

By field solving the four-port simulation topology depicted in Figure 3 and differential mode conversion, far-end crosstalk of the transmission line models in Table 2 are plotted in Figure 4 (i.e., from 1MHz to 30GHz). Across the wideband up to 30GHz, crosstalk for model 3A is about 3dB lower versus 3B. Similarly, crosstalk for model 4A is at least 2.5dB lower versus 4B. This result indicates

that for both microstrip and stripline in differential mode, thinner substrate or dielectric between a PCB trace and an adjacent reference plane reduces the signal crosstalk.

## Summary

The study presented here proves that crosstalk can be minimized by reducing the dielectric thickness between a PCB trace and the adjacent reference plane. This simple implementation serves as

an additional way to further reduce unintentional coupling, alongside other good PCB layout practices such as increasing the coupled distance and decreasing the coupled length between adjacent transmission lines. **DESIGN007**

## References

1. Barry Olney, Beyond Design, [Signal Integrity, Part 2](#), November 2014.
2. Altera, [High-Speed Board Layout Guidelines](#).



**Chang Fei Yee** is a hardware engineer with Keysight Technologies. His responsibilities include embedded system hardware development, and signal and power integrity analysis.

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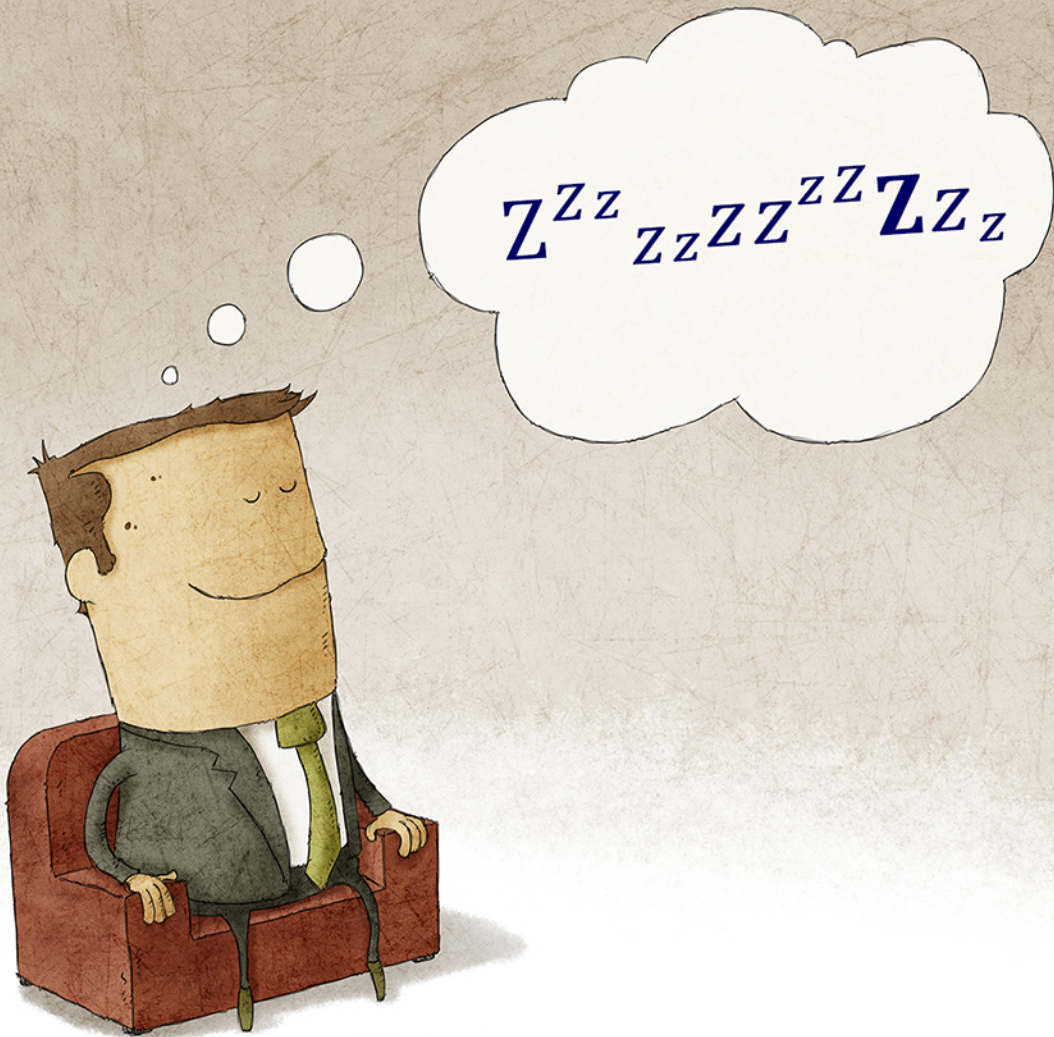
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The presenter is Kyle Lake of Oasis Sales, formerly a corporate marketing engineer with Mentor.

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# Moving From 28 Gbps NRZ to 56 Gbps PAM-4: Is it a Free Lunch?

Article by Yuriy Shlepnev  
SIMBERIAN INC.

The usual way of signaling through PCB interconnects is a two-level pulse, an encoding of 1s and 0s or bits, named NRZ (non-return-to-zero) or PAM-2 line code type. Increasing the data rate with the NRZ code type presents some obstacles. For a 28 Gbps NRZ signal, the bit time is about 35.7 ps with the main spectral lobe below 28 GHz. For a 56 Gbps NRZ signal, the bit time is about 17.86 ps, with the main spectral lobe below 56 GHz.

One can feel the problem already: Getting PCB interconnect analysis and measurements up to 56 GHz and beyond is very challenging, to say the least. In addition, the expected attenuation (dielectric, conductor and roughness losses) would also be an obstacle for 56 GHz NRZ. To reduce the bandwidth of the signal, pulse amplitude modulation with four levels (PAM-4) is being used more frequently on production boards.

Instead of single bits, symbols 00, 01, 10, and 11 are coded by four levels of the pulse and the symbol time is twice as large as the bit time for NRZ signal with the same data rate; that is about 35.7 ps for 56 Gbps PAM-4—the same as for 28 Gbps NRZ! If we know how to design interconnects that correlate with the measurements for 28 Gbps NRZ, is it going to be a free lunch to move to 56 Gbps NRZ?

It's not so easy, as I learned from Alex Manukovsky's tutorial, "A step by step guide for channel modeling and simulation that correlate to lab measurement for 25 Gb NRZ & 56 Gb PAM-4 applications" and the panel discussion, "The Case of the Closing Eyes: Is PAM the

Answer? Is NRZ dead?" at DesignCon 2018. So, to look into this problem, I decided to do a numerical experiment and compare the predictability of the interconnects for NRZ and PAM-4 signals of the test board EvR-1 featured in our DesignCon 2018 paper ["40 GHz PCB Interconnect Validation: Expectations vs. Reality,"](#) co-written with Marko Marin of Infinera.

We used the "sink or swim" formula for predictable interconnect design. It is based on three components: interconnect geometry adjustments + identified material models + validated software -> predictable interconnects. With all three components in place, we were able to reliably predict behavior of most of the interconnect structures on the EvR-1 board without additional tuning or calibration for the 28-30 Gbps NRZ signal.

For instance, Figure 1 depicts a simple differential link with two segments of 1.1"

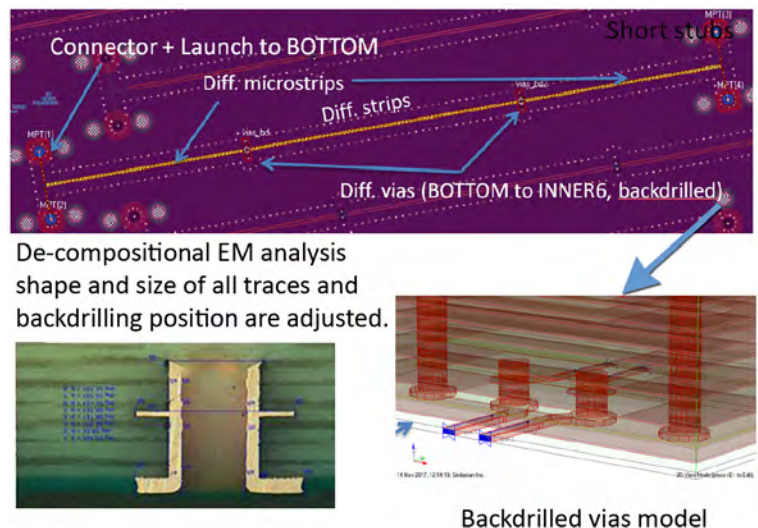


Figure 1: A simple differential link shows how to reliably predict behavior.

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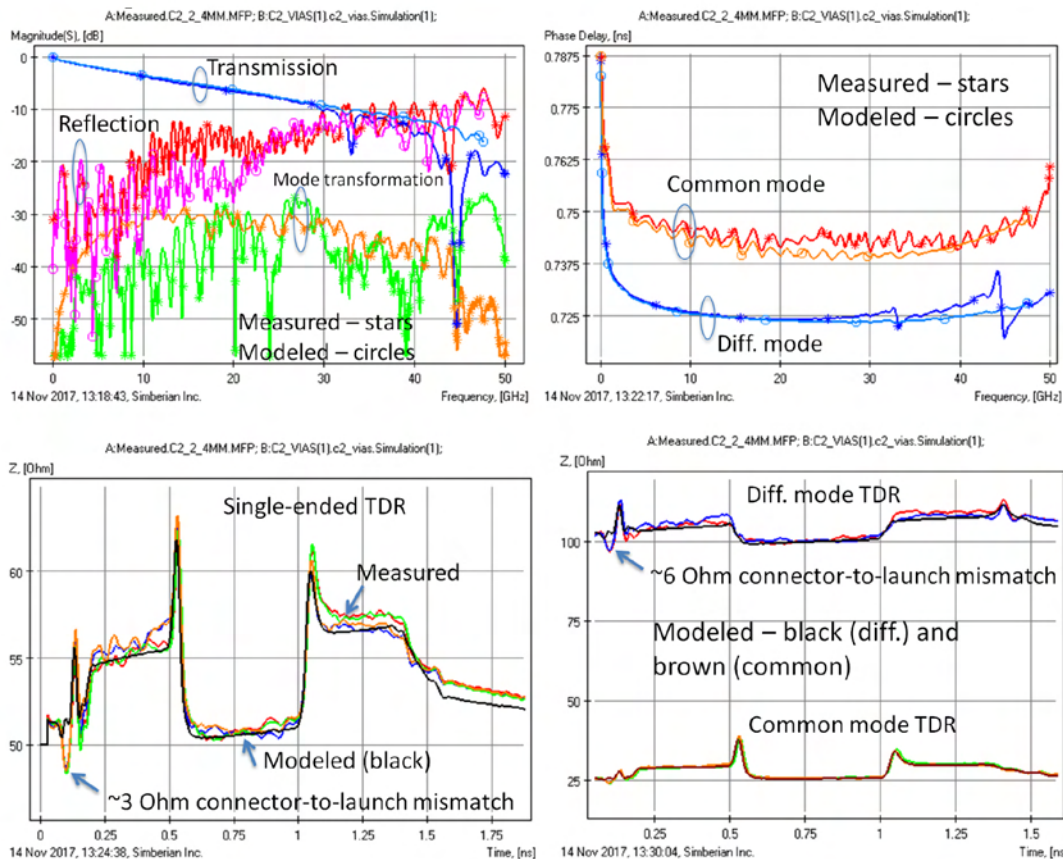
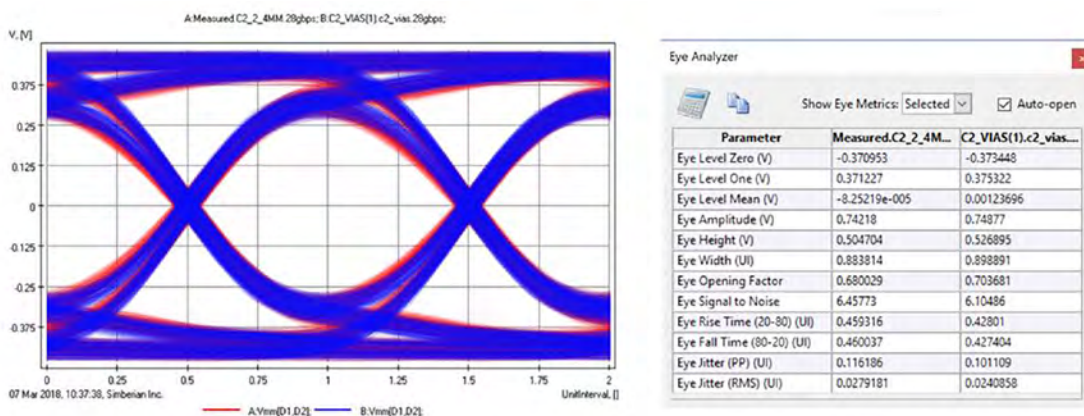


Figure 2: Analysis-to-measurement correlation in frequency domain is acceptable up to 30 GHz.

microstrip line, two pairs of back-drilled vias, 1.5" of stripline and four press-fit connectors and launches to do the measurements.

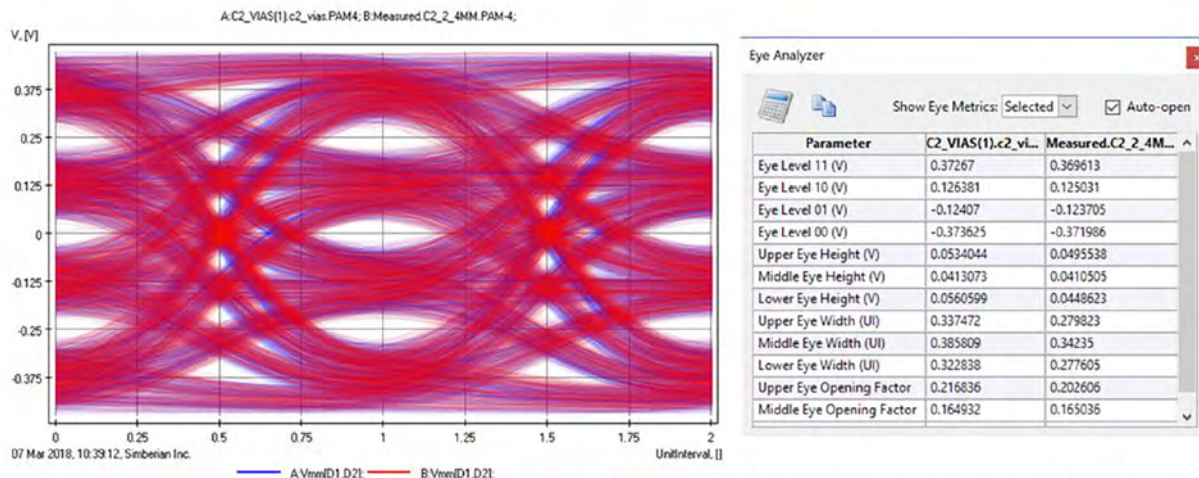
The vias, trace size and shapes are adjusted to match the actual manufactured structures (remember, the boards are not manufactured as designed). The dielectric and conductor roughness models are identified with S-param-

eters measured for two differential microstrip and two differential stripline segments using the generalized modal S-parameters (GMS-parameters) technique with proper loss dielectric and conductor loss separation (see details in the paper). As shown in Figure 2, the analysis-to-measurement correlation in frequency domain was acceptable up to 30 GHz and TDR



28 Gbps NRZ: model – blue, measured – red; 5.5% difference in eye heights and 1.5% in heights

Figure 3: The correlation is used to reliably predict the eye diagram for the 28 Gbps NRZ signal.



56 Gbps PAM-4: model – blue, measured – red; up to 25% difference in eye heights and 20% in widths

Figure 4: Moving from 28 Gbps to 56 Gbps raises the NRZ error to about 25%.

showed variations consistent with the low-cost PCB interconnects.

This correlation was sufficient to reliably predict the eye diagram for the 28 Gbps NRZ signal as seen in Figure 3 (15 ps rise and fall time, PRBS-32).

A 5.5% difference in the eye heights and just 1.5% in eye widths is not bad, considering the low-cost manufacturing very similar to the production boards. Now, let's try to predict 56 Gbps PAM-4 with the same 15 ps rise and fall time and PRBS-32.

Notice in Figure 4 that the relatively small amplitude error in the case of NRZ is now about a 25% error! The eye width is not predicted accurately either. What is the problem? Obviously, we have smaller eye openings for three eyes and, naturally, the relative error increased. In Figure 5, let's look at the spec-

tra of the signals used to generate these eye diagrams (computed with DFFT for the finite sequence of bits and symbols).

The NRZ signal in this case has about twice the power compared to the PAM-4 signal with the double data rate and the same rise/fall time and the same amplitude. The ratio of the power in the second lobe to the first one is about the same for both signal types. The bit time of the 28 Gbps NRZ signal is equal to the symbol time of the 56 Gbps PAM-4 signal. The accuracy of the analysis for both signals depends on the accuracy of the model above 28 GHz, that is where the second lobe of the spectrum is located. The model in this case does not correlate with the measurements above about 30 GHz due to the loss of the localization properties by the vias. This inaccuracy did not prevent acceptable correlation for the 28

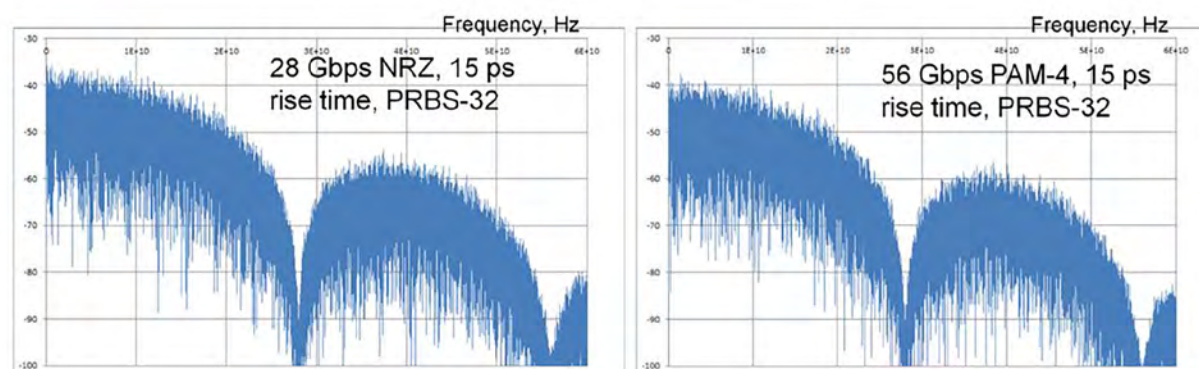


Figure 5: The spectra of the signals used to generate these eye diagrams.

Gbps NRZ signal. However, it degraded the accuracy of the model with 56 Gbps PAM-4, and it looks like the signal energy above 28 GHz is more important to account for in this case, in order to have the analysis that correlates with the measurements. The absence of the correlation would probably not prevent the link operation in this case; the slight eye degradation will be handled by the adaptive Rx/Tx. This may be different for links at the border of the Tx/Rx compliance margins.

The bottom line is that the modeling of PAM-4 links with double data rates is more challenging than for the NRZ. The correlation bandwidth of the models should be extended for PAM-4. This means that the design process must include manufacturing adjustments and material model identification, and, most importantly, the interconnect analysis software should be validated up to 40-50 GHz for 56 Gbps PAM-4 links.

It may sound ridiculous, but most of the interconnect analysis tools are not validated and, moreover, cannot be validated. The key in the validation is to make the minimal number of initial steps (geometry adjustments and material model identification) and apply the tool to typical interconnect structures without further adjustments. This is how we introduced the CMP-28 board with Wild River Technology about five years ago and demonstrated on EvR-1 board with Marko Marin at DesignCon 2018.

This is all about building the process and validating the tools. Do not trust the tool vendors just because you paid a lot for the tool or it's described as "3D electromagnetic," or the marketing manager says that the tool is accurate and even "intelligent" and validated, even if he shows you a couple of cases.

Trust, but validate everything! **DESIGN007**



**Yuriy Shlepnev** is founder and president of Simberian Inc.

## Novel Approach to Coherent Control of a Three-Level Quantum System

For the first time, researchers were able to study quantum interference in a three-level quantum system and thereby control the behavior of individual electron spins. To this end, they used a novel nanostructure, in which a quantum system is integrated into a nanoscale mechanical oscillator in form of a diamond cantilever. Nature Physics has published the study that was conducted at the University of Basel and the Swiss Nanoscience Institute.

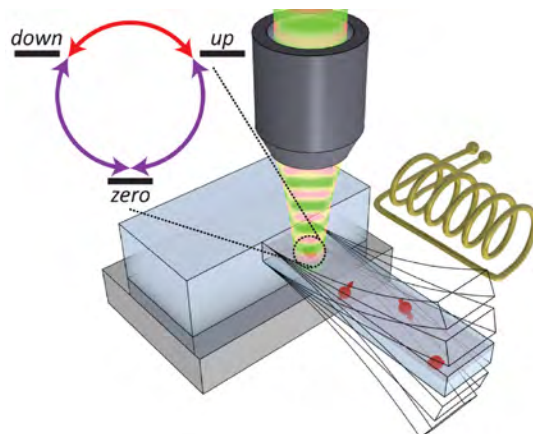
The electronic spin is a fundamental quantum mechanical property intrinsic to every electron. In the quantum world, the electronic spin describes the direction of rotation of the electron around its axis which can normally occupy two so-called eigenstates commonly denoted as "up" and "down." The quantum properties of such spins offer interesting perspectives for future technologies, for example in the form of extremely precise quantum sensors.

Researchers led by Professor Patrick Maletinsky and PhD candidate Arne Barfuss from the Swiss Nanoscience Institute at the University of Basel report in Nature Physics a new method to control the spins' quantum behavior through a mechanical system.

For their experimental study, they combined such a quantum system with a mechanical oscillator. More specifically, the researchers employed electrons trapped in so-called nitrogen-vacancy centers and embedded these spins in single-crystalline mechanical resonators made from diamond.

In particular, the oscillator allowed them to address all three possible transitions in the spin and to study how the resulting excitation pathways interfere with each other.

Source: University of Basel





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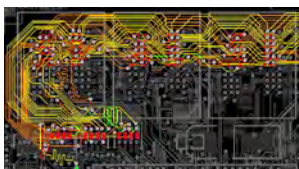
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# TOP 10

## Recent Highlights from Design007

### 1 DDR3/4 Fly-by Topology Termination and Routing ►

If you are employing high-frequency DDR4, then the bandwidth of the channel needs to be as high as possible. However, with today's extremely fast edge rates, the sequencing of the stubs and the end termination, and the associate load, can make a measurable difference in signal quality. In this month's column I will look at how best to route DDR3/4 fly-by topology.



### 3 Help Wanted: PCB Design Layout Specialist ►

I wish to reassure my fellow designers as you read this article that, in my opinion, you are in the catbird seat. You are in **hot** demand and you should have great opportunities for the remainder of your career. By the way, after reading this article, you may feel empowered to go ask for a raise. Please don't tell your manager that I sent you!



### 2 Siemens and Synopsys Team Up to Expand and Extend EDA Collaboration ►

Siemens PLM Software and Synopsys have agreed to collaborate on a wide range of electronic design automation (EDA) product interoperability projects for the benefit of their mutual customers. The collaboration spans a number of EDA domains from design to verification.

### 4 ANSYS Reports Strong Revenue and Earnings Growth in Q2 2018 ►

ANSYS reported second quarter 2018 GAAP and non-GAAP revenue growth of 11% and 13%, respectively, or 9% and 10%, respectively, in constant currency. Recurring revenue, which comprises lease license and annual maintenance revenue, totaled 76% of revenue for the second quarter on both a GAAP and non-GAAP basis.

## 5 Advanced Stackup Planning with Impedance, Delay and Loss Validation ▶

A typical PCB design usually starts with the material selection and stackup definition—the stackup planning or design exploration stage. How reliable are the data provided by the material vendors and PCB manufacturers? Can we use these data to predict trace width and spacing for the target trace impedance or to calculate delays or evaluate the loss budget?



## 6 EMA Expands Library with Power Integrations EDA and MCAD Models ▶

EMA Design Automation announced the availability of symbols, footprints, and 3D models for all Power Integrations components, which anyone can access for free from [ultralibrarian.com](http://ultralibrarian.com), [power.com](http://power.com), and [digikey.com](http://digikey.com). “With this new set of models, engineers can simply download the library components they need for their Power Integrations based designs,” said Manny Marciano, president and CEO of EMA.

## 7 Susy Webb: Training the New Generation of Designers ▶

In this conference call with I-Connect007 Editors Happy Holden and Patty Goldman, I asked Susy to discuss the next generation of PCB designers, some of the trends she’s seeing among new PCB designers, and the need for designers to take charge of their own design training, whether their management agrees or not.

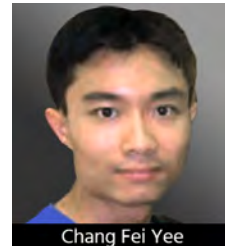


## 8 Irridian Invests in New Printed Circuit Board Design Software Suites ▶

Recently acquired by Hindley Circuits, Irridian Industrial Electronics, has invested in introducing state-of-the-art PCB design software to significantly enhance the accuracy and speed of its design services. The new Zuken CADSTAR and Altium design software platforms have modern and interactive user interfaces.

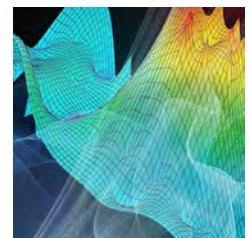
## 9 Achieving Optimum Signal Integrity During Layer Transition on High-Speed PCBs ▶

This article discusses the impact of stitching vias and discontinued return path or reference on signal integrity during layer transition on high-speed PCBs, particularly in terms of signal reflection and crosstalk.



## 10 Cadence Sigrity 2018 Release Accelerates PCB Design Cycles ▶

Cadence Design Systems has launched Cadence Sigrity 2018, which includes new 3D capabilities that enable PCB design teams to accelerate design cycles while optimizing cost and performance. A unique, 3D design and 3D analysis environment integrating Sigrity tools with Cadence Allegro technology provides a more efficient and less error-prone solution than current alternatives utilizing third-party modeling tools.



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# Career Opportunities



## Product Group Field Manager Waterbury, CT

Do you have what it takes? MacDermid Enthone Electronics Solutions is a leading supplier of specialty chemicals, providing application-specific solutions and unsurpassed technical support.

The position of the Product Group Field Manager will be responsible for creating and driving a strategic plan for the regional product line, including the following:

- Possess a thorough understanding of the overall PCB business, and specifics in wet processing areas
- Play an integral part in developing a commercial and technical customer strategy
- Create and deliver customer facing presentations
- Provide technical training for field staff
- Create and execute a product rationalization program
- Develop new product roll-out packages

### Hiring Profile

- Bachelor's Degree or 5 years' job-related experience
- Strong understanding of chemistry and chemical interaction within PCB manufacturing
- Excellent written and oral communication skills
- Strong track record of navigating technically through complex organizations
- Willingness to travel

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## General Manager - Operations, Germany

We are looking for an experienced and commercially-minded General Manager of Operations to join our team at our German facility in Kirchheimbolanden. This position has become available following our recent Taiwanese Stock Market listing, significant rise in demand, increasing market share and growing world-wide operations.

As General Manager - Operations you will strategically manage and oversee operations at the Kirchheimbolanden facility to maximize the efficiency and effectiveness of stock handling, production and warehousing in a world-class operation. Your primary responsibilities will include team leadership, strategic business planning, financial reporting, and quality control to ensure that the requirements of the business for fast turn delivery of quality products is met at the lowest possible cost.

### Skills and abilities required for the role:

- Proven commercial experience in similar manufacturing businesses. PCB or electronics industry background an advantage
- Strong organisational, time, and people management skills
- Strong interpersonal skills
- Financial literacy
- A commitment to highest quality customer service
- Excellent English language communication skills

You will be a core member of the management team reporting to the COO EMEA & USA.

- Excellent salary & benefits commensurate with experience
- Relocation package available for right candidate

Please forward your resume to  
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# Career Opportunities



## Role: Vice President Gardien Taiwan TAOYUAN COUNTY, TAIWAN

Gardien Taiwan is a service provider of circuit board (PCB) quality solutions, including electrical testing, AOI optical inspection, engineering (CAM), fixture making, repair and rework. Gardien Taiwan operates service centers in Taoyuan and employs about 100 employees and is currently seeking a vice president to manage and oversee the entity.

### Candidate Profile:

- Proficiency in Chinese and English (written and spoken)
- Excellent communication and organization skills
- Experience in change management
- PCB background appreciated, but not mandatory
- Management experience in internationally operating companies
- Savvy in standard office software (Word, Excel and Power Point)

If this sounds like you, please [click here](#) to send us an email with your attached CV.

About Gardien Group - Gardien is the world's largest international provider of independent testing and QA solutions to the PCB industry with a global footprint across 24 service centres in five countries and we cater to a whole range of customers, from small family owned PCB shops to large international fabricators. Gardien's quality solutions and process standards are trusted by leading high-tech manufacturers and important industries including aerospace, defense, and medical technology.

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# ZENTECH

## Zentech Manufacturing: Hiring Multiple Positions

Are you looking to excel in your career and grow professionally in a thriving business? Zentech, established in Baltimore, Maryland, in 1998, has proven to be one of the premier electronics contract manufacturers in the U.S.

Zentech is rapidly growing and seeking to add Manufacturing Engineers, Program Managers, and Sr. Test Technicians. Offering an excellent benefit package including health/dental insurance and an employer-matched 401k program, Zentech holds the ultimate set of certifications relating to the manufacture of mission-critical printed circuit card assemblies, including: ISO:9001, AS9100, DD2345, and ISO 13485.

Zentech is an IPC Trusted Source QML and ITAR registered. U.S. citizens only need apply.

Please email resume to  
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# Career Opportunities



## Sales Associate - Mexico

Manncorp, a leader in the electronics assembly industry for over 50 years, is looking for an additional sales associate to cover all of Mexico and to be part of a collaborative, tight-knit team. We offer on-the-job training and years of industry experience in order to set up our sales associate for success. This individual will be a key part of the sales cycle and be heavily involved with the customers and the sales manager.

### Job responsibilities:

- Acquire new customers by reaching out to leads
- Ascertain customer's purchase needs
- Assist in resolving customer complaints and queries
- Meet deadlines and financial goal minimums
- Make recommendations to the customer
- Maintain documentation of customer communication, contact and account updates

### Job requirements:

- Located in Mexico
- Knowledge of pick-and-place and electronics assembly in general
- 3+ years of sales experience
- Customer service skills
- Positive attitude
- Self-starter with ability to work with little supervision
- Phone, email, and chat communication skills
- Persuasion, negotiation, and closing skills

### We offer:

- Competitive salary
- Generous commission structure

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## Technical Support Engineer, Germany

We are looking for a Technical Support Engineer to join our team at our German facility in Kirchheimbolanden. The successful candidate will assist potential customers and current customers in appreciating the benefits of using—and optimizing the use of—Ventec materials in their printed circuit board manufacturing processes, and so enhance customer loyalty and satisfaction, spread the use of Ventec materials, and grow sales. The Technical Support Engineer will provide a two-way channel of technical communication between Ventec's production facilities and UK/European customers.

### Skills and abilities required for the role:

- Scientific/technical educational background.
- Experience in the PCB industry in engineering and/or manufacturing
- Good communications skills (German and English), able to write full technical reports for group or customer distribution.
- Ability to work in an organized, proactive, and enthusiastic way.
- Ability to work well both in a team as well as an individual.
- Good user knowledge of common Microsoft Office programs.
- Full driving license essential.
- Willingness to travel regularly throughout Europe and occasionally to Asia.

### What we offer:

- Excellent salary & benefits commensurate with experience

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# Career Opportunities



## IPC Master Instructor

This position is responsible for IPC and skill-based instruction and certification at the training center as well as training events as assigned by company's sales/operations VP. This position may be part-time, full-time, and/or an independent contractor, depending upon the demand and the individual's situation. Must have the ability to work with little or no supervision and make appropriate and professional decisions. Candidate must have the ability to collaborate with the client managers to continually enhance the training program. Position is responsible for validating the program value and its overall success. Candidate will be trained/certified and recognized by IPC as a Master Instructor. Position requires the input and management of the training records. Will require some travel to client's facilities and other training centers.

For more information, click below.

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# Mentor®

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## ***PCB Manufacturing, Marketing Engineer***

Use your knowledge of PCB assembly and process engineering to promote Mentor's Valor digital manufacturing solutions via industry articles, industry events, blogs, and relevant social networking sites. The Valor division is seeking a seasoned professional who has operated within the PCB manufacturing industry to be a leading voice in advocating our solutions through a variety of marketing platforms including digital, media, trade show, conferences, and forums.

The successful candidate is expected to have solid experience within the PCB assembly industry and the ability to represent the Valor solutions with authority and credibility. A solid background in PCB Process Engineering or Quality management to leverage in day-to-day activities is preferred. The candidate should be a good "storyteller" who can develop relatable content in an interesting and compelling manner, and who is comfortable in presenting in public as well as engaging in on-line forums; should have solid experience with professional social platforms such as LinkedIn.

Success will be measured quantitatively in terms of number of interactions, increase in digital engagements, measurement of sentiment, article placements, presentations delivered. Qualitatively, success will be measured by feedback from colleagues and relevant industry players.

This is an excellent opportunity for an industry professional who has a passion for marketing and public presentation.

Location flexible: Israel, UK or US

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# Career Opportunities



## SMT Field Technician Huntingdon Valley, PA

Manncorp, a leader in the electronics assembly industry, is looking for an additional SMT Field Technician to install and support our wide array of SMT equipment.

### Duties and Responsibilities:

- Manage on-site installation of equipment and training of customers
- Troubleshoot and diagnose technical problems by phone, email or additional on-site visits, when necessary during post-installation service and support
- Assist with demonstrations of equipment to potential customers
- Build and maintain positive relationships with customers
- Produce service reports
- Cooperate with technical team and share information across the organization
- Assist with the crating and uncrating of equipment

### Requirements and Qualifications:

- Three to five years of experience with SMT equipment, or equivalent technical degree
- Strong mechanical and electrical troubleshooting skills
- Proficiency in reading and verifying electrical, pneumatic, and mechanical schematics/drawings
- Organizational skills, detail oriented and capable of multitasking
- Good written and oral interpersonal skills with an ability to work under minimum supervision
- Ability to work with little supervision while traveling
- Availability for frequent travel
- Ability to arrange and schedule service trips
- USA Citizenship required

### We Offer:

- Health & dental insurance
- Retirement fund matching

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## Technology Communications Writer/Content Manager Board Systems Division

Mentor Graphics, a Siemens business, is a global technology leader in EDA software, enabling global companies to develop new and highly innovative electronic products in the increasingly complex world of chip, board, and system design.

### Job Duties:

The Mentor printed circuit board (PCB) technical writer/content manager will:

- Write and produce high-quality content for various properties (blogs, product collateral, technical white papers, case studies, industry publications, etc.)
- Gather research and data, interview subject matter experts, and transform complex information into clear, concise marketing communications
- Manage projects across multiple PCB product teams (high-speed design/analysis, advanced packaging, board design) within a deadline-driven environment

### Job Qualifications:

The ideal candidate should possess:

- Strong writing and editing skills with experience in PCB design technologies
- Desktop publishing skills (InDesign) using project templates and knowledge of online publications and social media
- A technical background (B.S. in electrical engineering or computer science preferred; this role works closely with the PCB division's technical marketing engineers and managers)
- Solid project planning and management skills; appreciation for adhering to deadlines; creativity for turning technical information into compelling content; teamwork and strong interpersonal communications skills; ability to be a self-starter

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September 11–13, 2018  
Santa Clara, California, USA

## **IPC E-Textiles 2018 Workshop** ▶

September 13, 2018  
Des Plaines, Illinois, USA

## **electronica India & productronica India** ▶

September 26–28, 2018  
Bengaluru, India

## **electronicAsia 2018** ▶

October 13–16, 2018  
Hong Kong

## **SMTA International** ▶

October 16–17, 2018  
Rosemont, Illinois, USA

## **TPCA Show 2018** ▶

October 24–26, 2018  
Taipei, Taiwan

## **electronica 2018** ▶

November 13–16, 2018  
Munich, Germany

## **HKPCA/IPC International Printed Circuit & South China Fair** ▶

December 5–7, 2018  
Shenzhen, China

## **48<sup>th</sup> NEPCON JAPAN** ▶

January 16–18, 2019  
Tokyo Big Sight, Japan

## **IPC APEX EXPO Conference and Exhibition** ▶

January 26–31, 2019  
San Diego, California, USA

## **DesignCon 2019** ▶

January 29–31, 2019  
Santa Clara, California, USA

## Additional Event Calendars



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barry@iconnect007.com

SALES MANAGER: **BARB HOCKADAY**  
(916) 608-0660; barb@iconnect007.com

MARKETING SERVICES: **TOBEY MARSICOVETERE**  
(916) 266-9160; tobey@iconnect007.com

EDITORIAL:  
MANAGING EDITOR: **ANDY SHAUGHNESSY**  
(404) 806-0508; andy@iconnect007.com

TECHNICAL EDITOR: **PETE STARKEY**  
+44 (0) 1455 293333; pete@iconnect007.com

MAGAZINE PRODUCTION CREW:  
PRODUCTION MANAGER: **SHELLY STEIN**  
shelly@iconnect007.com

MAGAZINE LAYOUT: **RON MEOGROSSI**

AD DESIGN: **SHELLY STEIN, MIKE RADOGNA ,**  
**TOBEY MARSICOVETERE**

TECHNOLOGY SPECIALIST: **BRYSON MATTIES**

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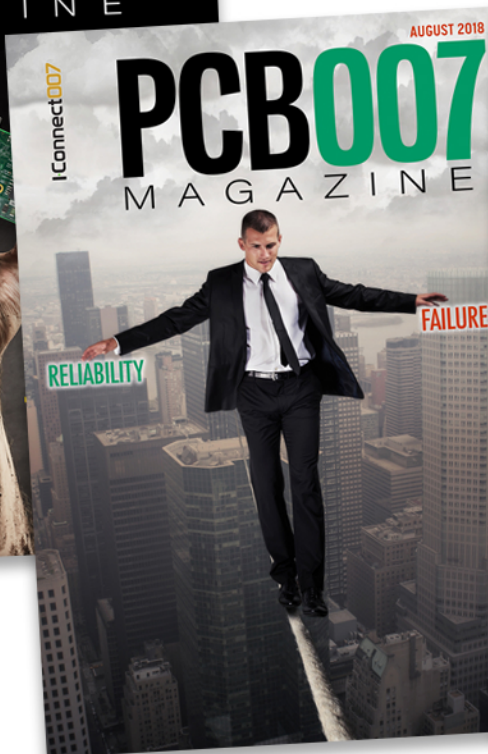
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## ADVERTISER INDEX

Accurate Circuit Engineering.....	5
Altium.....	41
American Standard Circuits.....	23
APCT.....	29
Candor Industries.....	11
Downstream Technologies.....	35, 69
Eagle Electronics.....	39
EMA Design Automation.....	15
Flex007 Magazine.....	72
General Circuits.....	17
I-Connect007 eBooks.....	2, 3
In-Circuit Design Pty Ltd.....	63
IPC.....	27
ITEQ.....	59
Mentor, a Siemens Business.....	49
Miraco.....	65
PCB007 China Magazine.....	79
Prototron Circuits.....	57
Pulsonix.....	19
Rogers Corporation.....	53
U.S. Circuit.....	43
Ventec International Group.....	7

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#### EDITORIAL CONTACT

**Andy Shaughnessy**

[andy@iconnect007.com](mailto:andy@iconnect007.com)

+1 404.806.0508 GMT-5



[mediakit.iconnect007.com](http://mediakit.iconnect007.com)

#### SALES CONTACT

**Barb Hockaday**

[barb@iconnect007.com](mailto:barb@iconnect007.com)

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